2.008 Design & Manufacturing II

Spring 2004

MEMS I

March 10th

- Ask “Dave” and “Pat”
  - Petty money up to $200, Goggles
  - Plant tour, April 21, 22, sign up! By 4/2
- Quiz 1 on March 17th
  - HW#4 due by Monday's lecture
  - 75 minutes (45 min)
- MEMS 1 today

Elephant vs. Ant

- Shock and impact
- Scale and form factor
- Load carrying capability
  - Spider silk v.s. steel

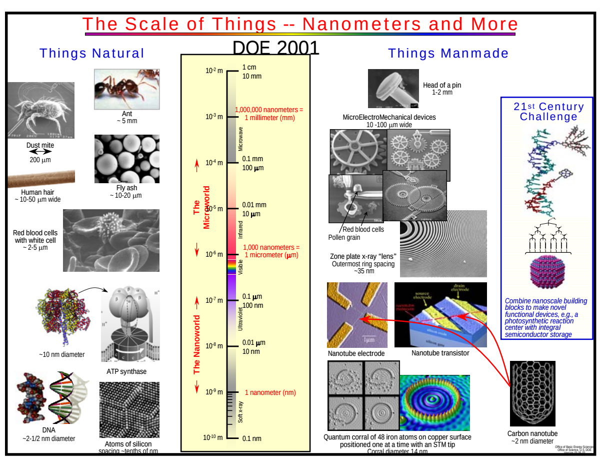
Frog, Water Strider, Gecko

Gecko adhesive system

Never try to mimic the nature.

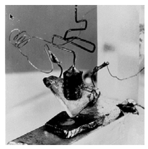
e.g. Biomimetic researches.

http://robotics.eecs.berkeley.edu/~ronf/GECKO/Figures/Hierarchy3.jpg



Transition: Micro to Nano

- 20th Century - Microelectronics and Information Technology
  - Semiconductors, computers, and telecommunication
- 21st Century - Limits of Microsystems Technology --- Nanotechnology
  - Moore's law
  - Hard disc drive

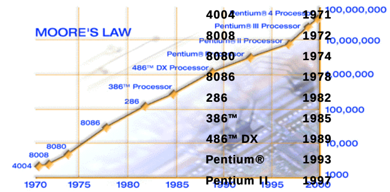


John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories, "First Transistor"

Moore's Law

The number of transistors per chip doubles every 18 months. – Moore's Law

_ Rock's Law



	Year of introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™	1985	275,000
486™ DX	1989	1,180,000
Pentium®	1993	3,100,000
Pentium II	1997	7,500,000
Pentium III	1999	24,000,000
Pentium 4	2000	42,000,000

Microelectronics Technology

To meet the Moore's Law,

line width(1/2 pitch) requirement

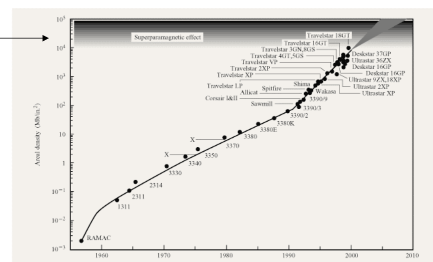
100 nm 2005
70 nm 2008
50 nm 2011
35 nm 2014

No solution yet, nanolithography?

G-line:436nm
I-line: 365nm
DUV: 248 nm
193 nm
EUV

The International Technology Roadmap for Semiconductors, 1999

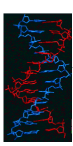
Aerial density, hard disk



- Superparamagnetic Effect

"a point where the data bearing particles are so small that random atomic level vibrations present in all materials at room temperature can cause the bits to spontaneously flip their magnetic orientation, effectively erasing the recorded data. "

What is Nanotechnology?



A DNA molecule is 2.5 nm wide.

Nanomanufacturing?

Nano in ME

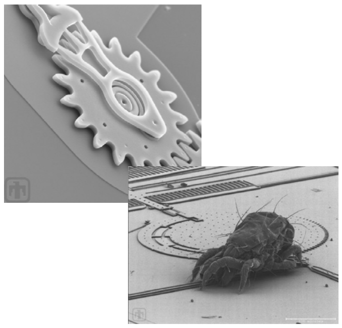
- Fluidics, heat transfer and energy conversion at the micro- and nanoscale
- Bio-micro-electromechanical systems (bio-MEMS)
- Optical-micro-electromechanical systems (optical-MEMS)
- Engineered nanomaterials
- Nano manufacturing
- Course 2A (Nanotrack)

http://www.memsnet.org/mems/what-is.html

MEMS

- Optical MEMS
- RF MEMS
- Data Storage
- Bio. MEMS
- Power MEMS
- MEMS for Consumer Electronics
- MEMS In Space
- MEMS for Nano.

▪Materials
▪Processes
▪Systems



Courtesy: Sandia national laboratory

MEMS (Microelectromechanical Systems)

- Intergrated systems of sensing, actuation, communication, control,power, and computing
- Tiny,
- Cheaper,
- Less power
- New functions!!! (chemical, bio, μ-fluidic, optical, ...)

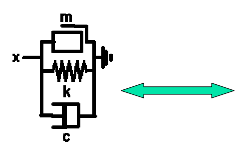
Tiny Products

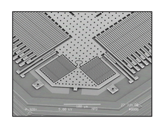
- DLP (Digital Micromirror Array)

DLP
10^6 micromirrors, each $16\mu m^2$, $\pm 10°$ tilt
(Hornbeck, Texas Instruments DMD, 1990)

Tiny Products

- Airbag sensors: Mechanical vs. MEMS

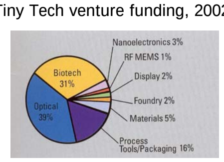




Tiny Products

- Airbag sensors: Mechanical vs. MEMS
- DLP (Digital Micromirror Array)
- DNA chip
- Optical MEMS

Tiny Tech venture funding, 2002



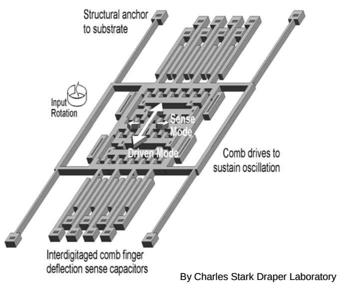
Smalltimes, Vol.2 , no. 6, 2002

(Courtesy of Segway (r) Human Transporter (HT). Used with permission.)

Segway

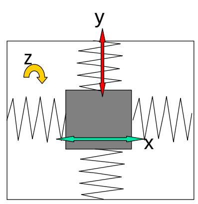
-Tilt
-Rotation

Vibrating Gyroscope



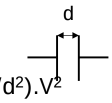
By Charles Stark Draper Laboratory

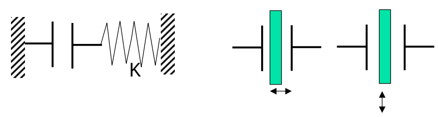
Coriolis Acceleration



Electrostatic Comb Drive/sensing

- Paralle Plate Capacitor
  - Capacitance=Q/V=ε A/d
    - ε Dielectric permittivity of air
  - Electrostatic Force = ½ ε (A/d^2).V^2
  - Pull-in point: 2/3 d

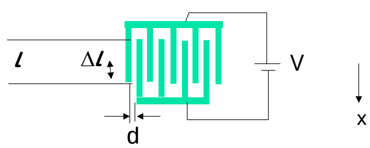




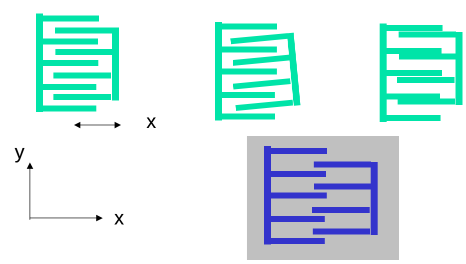
Comb Drive

- C= ε A/d = 2n ε *l* h/d
- ΔC = 2n ε Δ*l* h/d
- Electrostatic force

F_{el} = ½ *d*C/*dx* V^2 = n ε h/d V^2

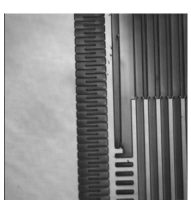


Suspension mode failures

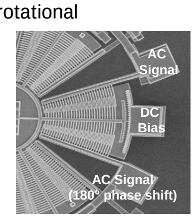


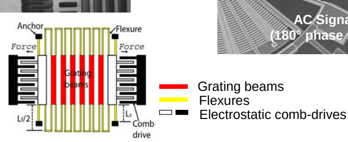
Comb Drive Designs

linear



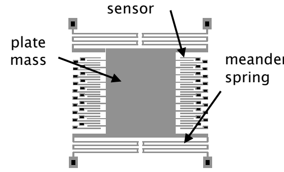
rotational

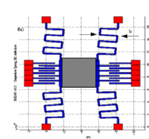




Grating beams
Flexures
Electrostatic comb-drives

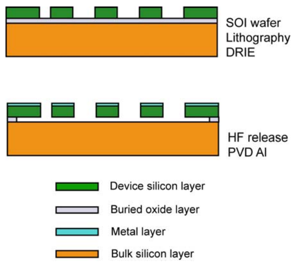
Capacitive Accelerometer





Microfabrication process flow

- Single-mask process
- IC compatible
- Negligible residual stress
- Thermal budget
- Not yet packaged

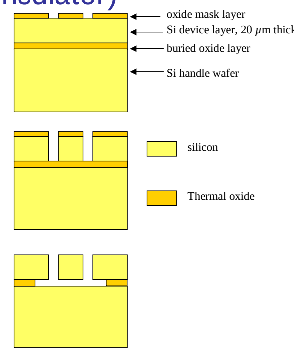


SOI (Silicon on insulator)

1) Begin with a bonded SOI wafer. Grow and etch a thin thermal oxide layer to act as a mask for the silicon etch.

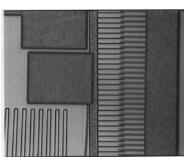
2) Etch the silicon device layer to expose the buried oxide layer.

3) Etch the buried oxide layer in buffered HF to release free-standing structures.



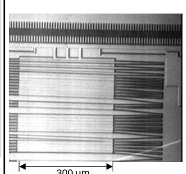
Problems of fabrication

Surface micromachined Structure 2 μm



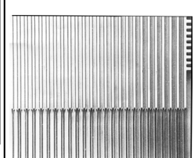
Vertical stiction

DRIE micromachined Structure 10 μm



Lateral stiction

DRIE micromachined Structure 10 μm

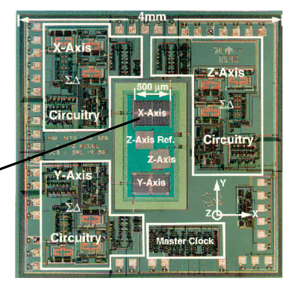


No stiction

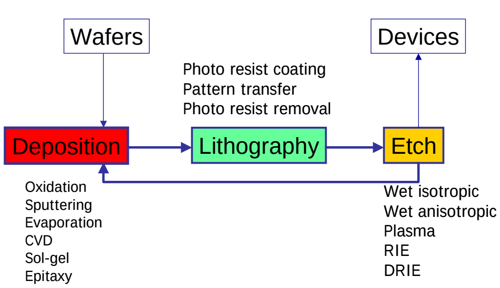
ADXL 50 accelerometer

Capacitive sensing

Comb drive



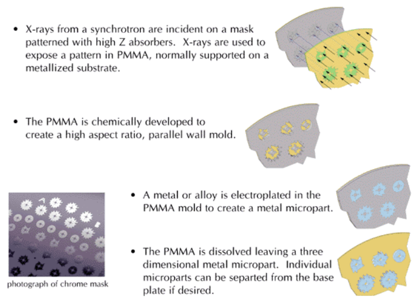
Process Flow



Micromachining processes

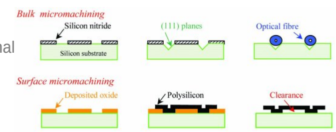
- Bulk micromachining
- Surface micromachining
- Bonding
- LIGA
  - x-ray lithography, electrodeposition and molding

LIGA process



Bulk, Surface, DRIE

- Bulk micromachining involves removal of the silicon wafer itself
  - Typically wet etched
  - Inexpensive equipments
  - IC compatibility is not good.
- Surface micromachining leaves the wafer untouched, but adds/removes additional thin film layers above the wafer surface.
  - Typically dry etched
  - Expensive equipments
  - IC compatibility, conditional



Materials

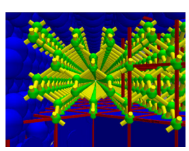
- Metals
  - Al, Au, ITO, W, Ni, Ti, TiNi,…
- Insulators
  - SiO_2 - thermally grown above 800ºC or vapor deposited (CVD), sputtered. Large intrinsic stress
  - Si_xN_y – insulator, barrier for ion diffusion, high E, stress controllable
- Polymers: PR, SU-8, PDMS
- Glass, quartz
- Silicon
  - stronger than steel, lighter than aluminum
  - single crystal, polycrystalline, or amorphous

Silicon

- Atomic mass average: 28.0855
- Boiling point: 2628K
- Coefficient of linear thermal expansion: 4.2. 10^{-6}/°C
- Density: 2.33g/cc
- Young's modulus: 47 GPa
- Hardness scale: Mohs' 6.5
- Melting point: 1683K
- Specific heat: 0.71 J/gK

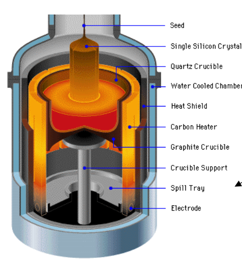
Electronic grade silicon
99.99999999% purity

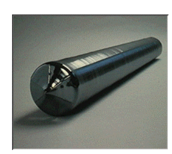
Materials



- Single crystal silicon
  - Anisotropic crystal
  - Semiconductor, great heat conductor
- Polycrystalline silicon – polysilicon
  - Mostly isotropic material
  - Semiconductor
- Semiconductor
  - Electrical conductivity varies over ~8 orders of magnitude depending on impurity concentration (from ppb to ~1%)
  - N-type and P-type dopants both give linear conduction.
- Two different types of doping
  - Electrons (negative, N-type) --phosphorus
  - Holes (positive, P-type) --boron

Silicon Ingot





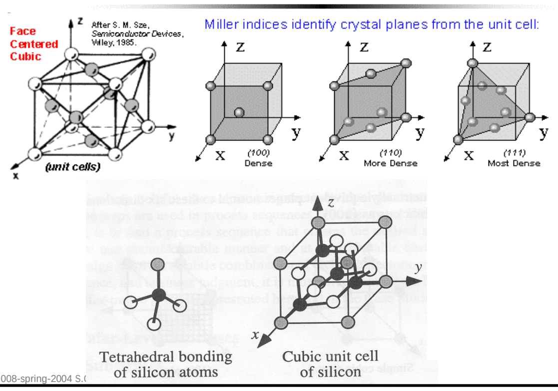
Czochralski (CZ) method

Float Zone (FZ) method.

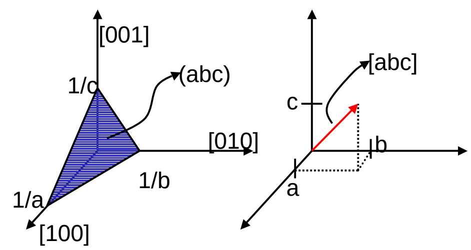
1" to 12" diameter

http://www.msil.ab.psiweb.com/english/msilhist4-e.html

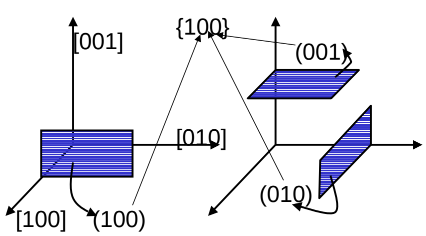
Silicon Crystal Structure



Miller indices, plane

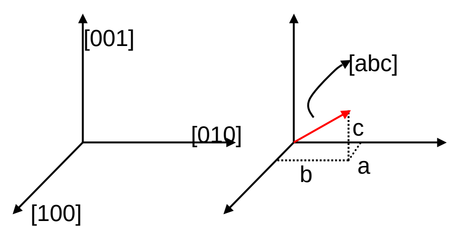


Crystallographic planes

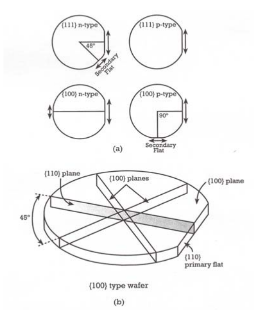


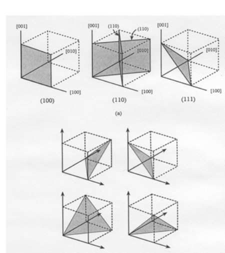
Miller indices

- [abc] in a cubic crystal is just a directional vector
- (abc) is any plane perpendicular to the [abc] vector
- (…)/[…] indicate a specific plane/direction
- {…}/<…> indicate equivalent set of planes/directions

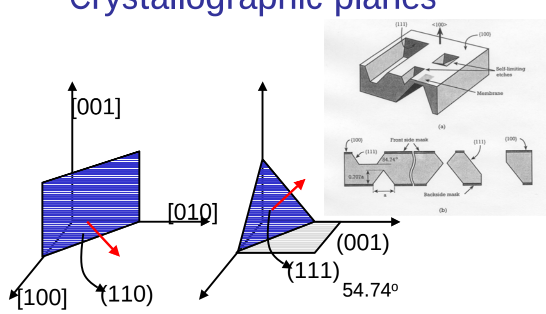


Wafers of different cuts





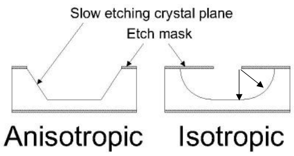
Crystallographic planes



Etching

Wet

Dry



- Isotropic silicon etchants
  - HNA ("poly-etch") -wet
    - Mix of HF, nitric acid (HNO_3), and acetic acids (CH_3COOH)
    - Difficult to control etch depth and surface uiformity
  - XeF_2 -dry
    - gas phase, etches silicon, polysilicon
    - Does not attack SiO2, SiNx,metals, PR

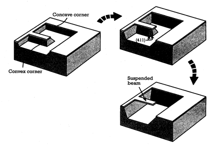
Anisotropic wet etching

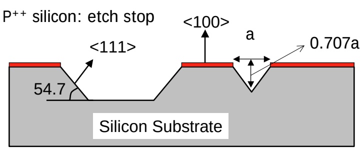
Many liquid etchants demonstrate dramatic etch rate differences in different crystal directions

- <111> etch rate is slowest, <100> fastest
- Fastest: slowest can be more than 100:1
- KOH, EDP, TMAH most common anisotropic silicon etchants
- Potasium Hydroxide (KOH), Tetramethyl Ammonium Hydroxide (TMAH), and Ethylene Diamine Pyrochatecol (EDP)

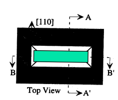
KOH Etching

- Etches PR and Aluminum instantly
- (100) to (111) → 100 to 1 etch rate
  - V-grooves, trenches
  - Concave stop, convex undercut
  - CMOS incompatible
- Masks:
  - SiO_2: for short period
  - Si_xN_y: Excellent
  - heavily doped P^{++} silicon: etch stop

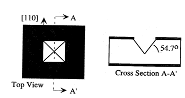




Anisotropic wet etching

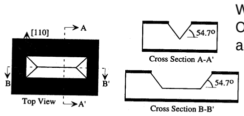


When a (100) wafer with mask features Oriented to <110> direction is placed in an anisotropic etchant.



A square <110> oriented mask feature results in a pyramidal pit.

Anisotropic wet etching



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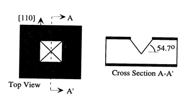
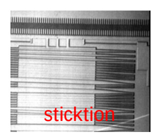


A square <110> oriented mask feature results in a pyramidal pit.

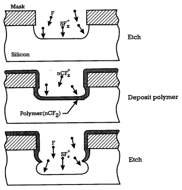
Dry etching



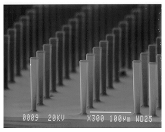
- RIE (reactive ion etching)
  - Chemical & physical etching by RF excited reactive ions
  - Bombardment of accelerated ions, anisotropic
  - SF6 → Si, CHF3 → oxide and polymers
  - Anisotropy, selectivity, etch rate, surface roughness by gas concentration, pressure, RF power, temperature control
- Plasma etching
  - Purely chemical etching by reactive ions, isotropic
- Vapor phase etching
  - Use of reactive gases, XeF2
  - No drying needed

DRIE (Deep RIE)

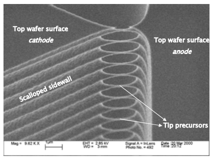
- Alternating RIE and polymer deposition process for side wall protection and removal
- Etching phase: SF_6 /Ar
- Polymerization process: CHF_3/Ar forms Teflon-like layer
- Invented by Bosch, process patent, 1994

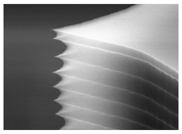


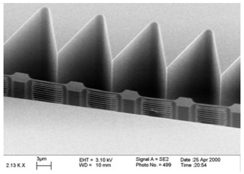
-1.5 to 4 μm/min
-selectivity to PR 100 to 1

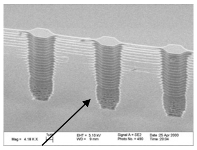


Scalloping and Footing issues of DRIE









Footing at the bottom of device layer

Milanovic et al, IEEE TED, Jan. 2001.

Deep Reactive Ion Etch

STS, Alcatel, Trion, Oxford Instruments …

Most wanted by many MEMS students

High aspect ratio 1:30

Easily masked (PR, SiO_2)