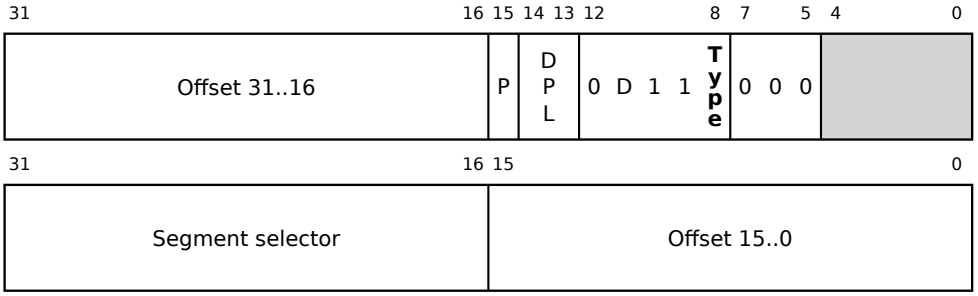
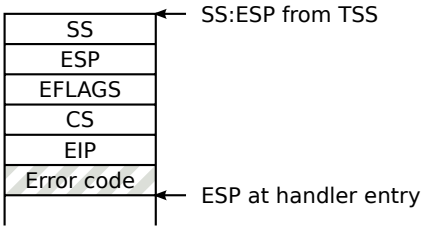
Interrupt/trap gate

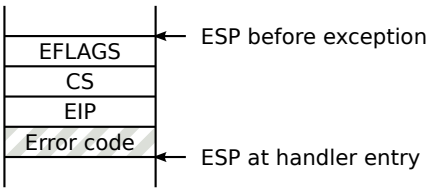


Type	0=Interrupt gate 1=Trap gate	P	Present
Selector	Destination CS	DPL	Descriptor privilege level (CPL required to invoke gate)
Offset	Destination IP or EIP	D	Size of gate (0=16-bits, 1=32-bits)

Exception stack (with privilege change)



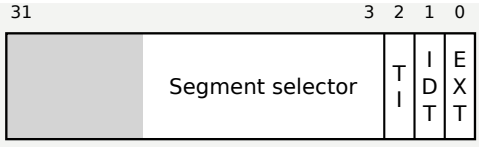
Exception stack (without privilege change)



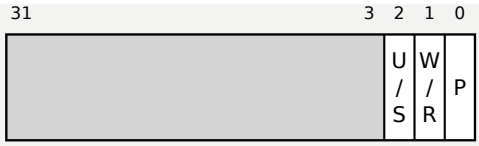
Vector	Description	Type	Error code
0	Divide error	Fault	No
1	Reserved		
2	Non-maskable interrupt	Interrupt	No
3	Breakpoint	Trap	No
4	Overflow	Trap	No
5	BOUND range exceeded	Fault	No
6	Invalid/undefined opcode	Fault	No
7	No math coprocessor	Fault	No
8	Double fault	Abort	Zero
9	Reserved		
10	Invalid TSS	Fault	Yes
11	Segment not present	Fault	Yes
12	Stack-segment fault	Fault	Yes
13	General protection	Fault	Yes
14	Page fault	Fault	Yes
15	Reserved		No
16	x87 FPU error	Fault	No
17	Alignment check	Fault	Zero
18	Machine check	Abort	No
19	SIMD FP exception	Fault	No
20-31	Reserved		
32-255	User defined interrupts	Interrupt	No

Exception types

Fault	Faulting instruction not executed CS:EIP is the faulting instruction
Trap	Trapping instruction executed CS:EIP is the next instruction
Abort	Location is imprecise; cannot safely resume execution



TI	0=GDT, 1=LDT
IDT	0=GDT/LDT, 1=IDT
EXT	External event



P	0=Non-present page 1=Protection-violation
W/R	Cause (0=Read, 1=Write)
U/S	Mode (0=Supervisor, 1=User)

6.828 Operating System Engineering

Fall 2012