

6.776

High Speed Communication Circuits
Spring 2005

Homework #3: High Speed Amplifiers

Passed Out: February 24, 2005 Due: March 3, 2005

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Reading: Chapters 3 and 8 and pages 280-283 of T. H. Lee's first edition book. These correspond to Chapters 5 and 9 and pages 375 (bottom of page) to 379 of his second edition book.

1. The following is based on Problem 8 in Chapter 8 of T.H. Lee's first edition book. Consider the zero-peaked amplifier shown in Figure 1.

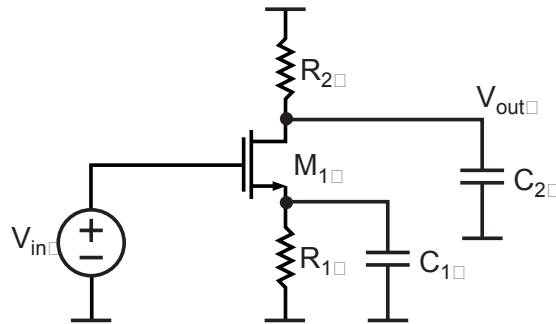


Figure 1: Zero-peaked amplifier.

- (a) Derive the transfer function expression for the small-signal gain from V_{in} to V_{out} . In your derivation, assume that M_1 is in saturation, and ignore C_{gd} , r_o , and backgate parasitics.
 - (b) Express the bandwidth of the amplifier as a function of the output pole, $1/(R_2C_2)$, under the assumption that $g_m R_1 = 10$ and C_1 is chosen such that the zero cancels the output pole in the gain expression derived above. Recognize that the output pole frequency corresponds to the bandwidth of the *unpeaked* amplifier.
2. The following is based on Problem 7 in Chapter 8 of T.H. Lee's first edition book. In general, high-speed followers, as shown in Figure 2, have a tendency to ring or even oscillate when driving certain loads. Your task is to identify the conditions that may cause this problem and to propose a solution. For derivations, ignore C_{gd} , r_o , and backgate parasitics of M_1 .

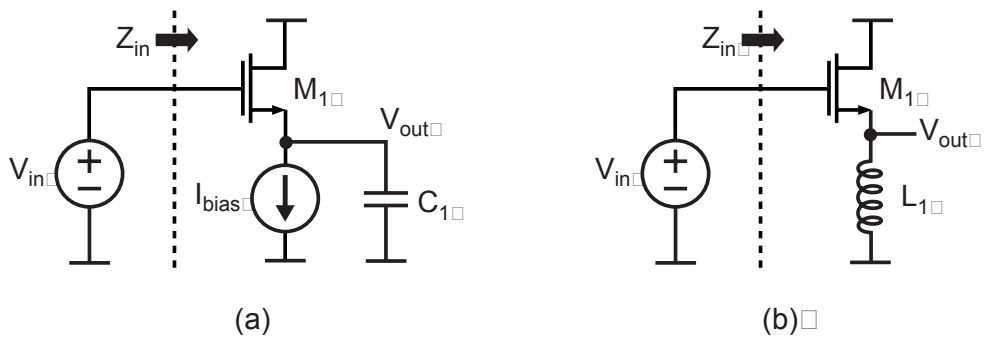


Figure 2: Source follower with a (a) capacitive load, (b) inductive load.

- (a) Consider the follower circuit in part (a) of the figure. Derive an expression for Z_{in} .
 - (b) Over what range of load capacitance can the real part of Z_{in} , as derived above, be negative? What is the impact of having the real part of the impedance become negative?
 - (c) Given that the load capacitance is chosen such that the real part of Z_{in} becomes negative, modify the circuit in part (a) of the figure such that the source V_{in} always sees an impedance whose real part is positive. In your design, be sure to preserve the high speed operation of the follower circuit, and provide formulas for the computation of the values of any components you add.
 - (d) Now consider the follower circuit with an inductor load in part (b) of the figure, whose analysis will also provide intuition of the impact of inductive source degeneration on CE and CS circuits. Derive an expression for Z_{in} under the assumption that C_{gd} and r_o of M_1 can be ignored. Examining the real part of the derived impedance, comment on whether ringing or oscillation problems can occur.
3. This problem focuses on the design of the broadband differential amplifier shown in Figure 3 based on the techniques described in class. Perform all computations based on the transistor models contained in the 0.18u Spectre model file provided on MIT server in the file `/mit/6.776/Models/0.18u/cmos018.scs`. For simplicity, assume all devices are the same size with transconductance g_m , all resistors are of the same value R , and that C_{fixed} , which corresponds to wiring capacitance, equals 10 fF.
- (a) Using Spectre and Matlab, plot the g_m versus I_d curve for a diode-connected NMOS device of width 1.8 microns and length 0.18 microns. The value of I_d should span from 0 to the value produced when V_{gs} equals 1.8 V. Use the appropriate Spectre commands to extract the g_m curve from the simulation as an ASCII file that is read in by Matlab.
 - (b) Compute the value of C_{gs} for the transistor in part (a) under the assumption that the NMOS device is in saturation.
 - (c) Write a Matlab script that determines the value of I_d at which the g_m curve generated in part (a) intersects with the line $2(A/V_{sw})I_d$, where A corresponds to

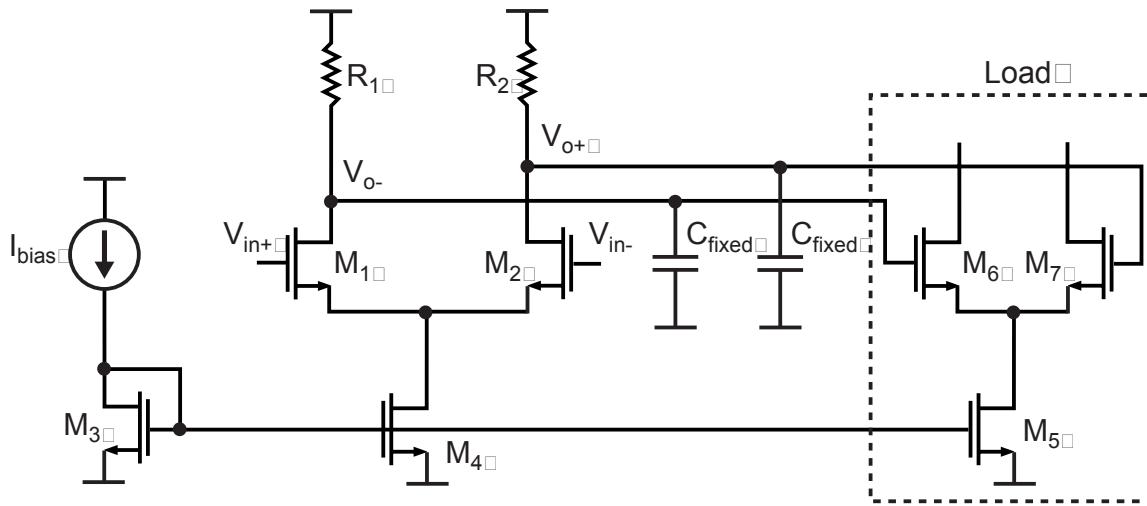


Figure 3: A high speed differential amplifier.

the single-ended amplifier gain ($g_m R$), and V_{sw} corresponds to the single-ended amplifier swing ($I_{bias} R$). State the values of I_d that result with $A = 3$ and $V_{sw} = 1$ V, for $A = 3$ and $V_{sw} = 0.5$ V, and for $A = 5$ and $V_{sw} = 1$ V.

- (d) Based on the results in part (c), compute the bandwidth of the amplifier for the case where $A = 3$ and $V_{sw} = 1$ V under the restriction that the device has a width of 1.8 microns and a length of 0.18 microns.
- (e) In the same manner as part (d), using the results of part(c), compute the bandwidth of the amplifier for the case where $A = 3$ and $V_{sw} = 0.5$ V under the restriction that the device has a width of 1.8 microns and a length of 0.18 microns. Comment on the results of parts (c) - (e).
- (f) Based on the results in part (c), what is the maximum bandwidth that can be achieved for $A = 3$ and $V_{sw} = 1$ V when the device size can be arbitrarily set? What is the penalty to achieving the maximum bandwidth?
- (g) In practice, a good compromise is to size the amplifiers such that their input load capacitance, i.e., C_{gs} , equals the fixed capacitance. Given this constraint, what is the appropriate device width and length, resistor load value R , and resulting bandwidth to achieve $A = 3$ and $V_{sw} = 1$ V? Comment on the rationale for this compromise.
- (h) Based on the insight gained in this problem, write a Matlab script that determines the maximum gain that can be achieved with a single-stage amplifier bandwidth of 2.5 GHz, 5 GHz, and 10 GHz. Assume that the devices are sized according to the constraint specified in part (g), and that $V_{sw} = 1$ V. State the values of gain that you achieve at each bandwidth setting.