6.772 Compound Semiconductor Devices

The Use of Strain in Silicon Germanium Heterostructure MOSFET technology

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Outline

- Motivation
- Bulk Si MOSFET overview
- Strained SiGe MOSFET overview
- Device physics of strain
- Impact on mobility
- Conclusion

Motivation

- Microprocessor design relies on CMOS digital integrated circuits.
  - low power
  - robust
- Si bulk CMOS scaling is reaching limit.
- Alternative techniques
  - Silicon-on-Insulator (SOI)
  - High-k gate dielectric
- Strained SiGe heterostructure MOSFET
  - “Strained Si” MOSFET

What's wrong with bulk Si MOSFETs?

- Performance improves as dimensions are scaled.
- Mobility imbalance
  - pMOS μ_{eff} 2X smaller than nMOS μ_{eff}
- Approaching physical limits to geometric scaling

$$I_{DS} \sim W C_{ox} f(\mu_{eff}; L_{eff})$$

$$C_{ox} \sim \frac{\varepsilon_{ox}}{t_{ox}}$$

→ **Concentrate to improving mobility, μ_{eff}.**

Strained SiGe MOSFET heterostructure

- $Si_{1-x}Ge_x$ layer strains top thin epitaxial Si layer
- Graded $Si_{1-x}Ge_x$ layer reduces threading dislocation density at the surface.

Why Silicon Germanium?

- Ge has indirect bandgap
- Low lattice mismatch
- Easy to integrate with Si MOSFETs

Physics of Strain

- Biaxial tensile and compressive strain distort energy bands.
- Significant impact on electronic properties.

Effects of Strain on Energy Bands

- Lattice distortion lifts degeneracies at band edges.

Effect on the Conduction Band

- Distortion lifts the six-fold degeneracy state, Δ_6, of the Si conduction band.
- During tensile strain
  - Lower energy - Δ_2
  - Higher energy - Δ_4
- Strain induced energy splitting is approximately 660 x (meV)

Effect on Conduction Band Con't

- Δ_2 band has lower effective mass associated with valley repopulation
  - Lowered by 2/3 ΔEs (Δ_4 raised by 1/3 ΔEs)
- Enhanced mobility for in-plane transport (for tensile strain)

Effect on Valence Band

- Unstrained Si suffers from high inter-valley scattering rates
- Biaxial tensile stress lifts the degeneracy of the valence band at k=0.
- Energy of heavy hole (HH) and spin-orbit (SO) subbands lowered relative to light hole (LH).
- Reduced inter-valley scattering
- Lower hole effective mass

Enhancement of Mobility

$$U = \frac{e \cdot t}{m^*}$$

- Carrier mobility is increased by:
  - reducing effective mass, *m*.*
  - increasing scattering time, *t* .
- Strained SiGe MOSFETs take advantage of both variables.

Mobility enhancements of Strained Si MOSFETs

- Electron and hole mobilities increase with tensile strain of Si
- Peak mobility enhancement ratio 1.8X for ~ 30% Ge substrate

Mobility enhancement vs. Ge Content

- Mobility enhancement ratio saturates with 30% Ge substrate.

MOSFET performance enhancements

- Surface-channel n-MOSFETs fabricated on $Si_{0.8}Ge_{0.2}$ substrates exhibit 60% enhancement in transconductance at a given channel length and power supply voltage.
- Enhancement achieved without degradation in short channel effects.

Conclusion

- Strained SiGe MOSFET extends fundamental scaling limit
- Unique electronic properties
- Enhanced mobility
  - Improved speed without short channel effects
- Future Work
  - Integrating SOI and high-K gate dielectric with Strained SiGe Heterostructure.

References

[1] J.L. Hoyt, 6.774: Physics of Microfabrication: Front End Processing, 2002.

[2] J.Welser,et al, IEDM Tech Dig.,p373(1994)

[3] K. Rim ,et al, IEDM Tech Dig.,p517(1995)

[4] J.L. Hoyt, Mat. Res. Soc.Symp. Proc. Vol. 387, pp. 299-310 (1995).

[5] A. Sadek, et al, IEEE Transactions on ,Volume: 43, 1996.

[6] K. Rim, et al,IEEE, Volume: 47 Issue: 7 , Jul 2000 Page(s): 1406 -1415.

[7] D.J. Paul, Thin Solid Films, 321 (1998) 172-180.

[8] J.L. Hoyt, et al, IEDM '02. Digest. International , 2002 Page(s): 23 -26.

[9] Xiangdong Chen, et al, IEEE, Sep 2001 Page(s): 1975 -1980.

[10] A. G. O'Neill; D.A. Antoniadis, IEEE, Jun 1996 Page(s): 911 -918

[11] C.W. Leitz, PHD thesis, MIT (2002).