Bipolar Junction Transistor Circuits
Biasing.

BJT Operating Regimes.

Let's start by reviewing the operating regimes of the BJT. They are graphically shown on Figure 1 along with the device schematic and relevant parameters.

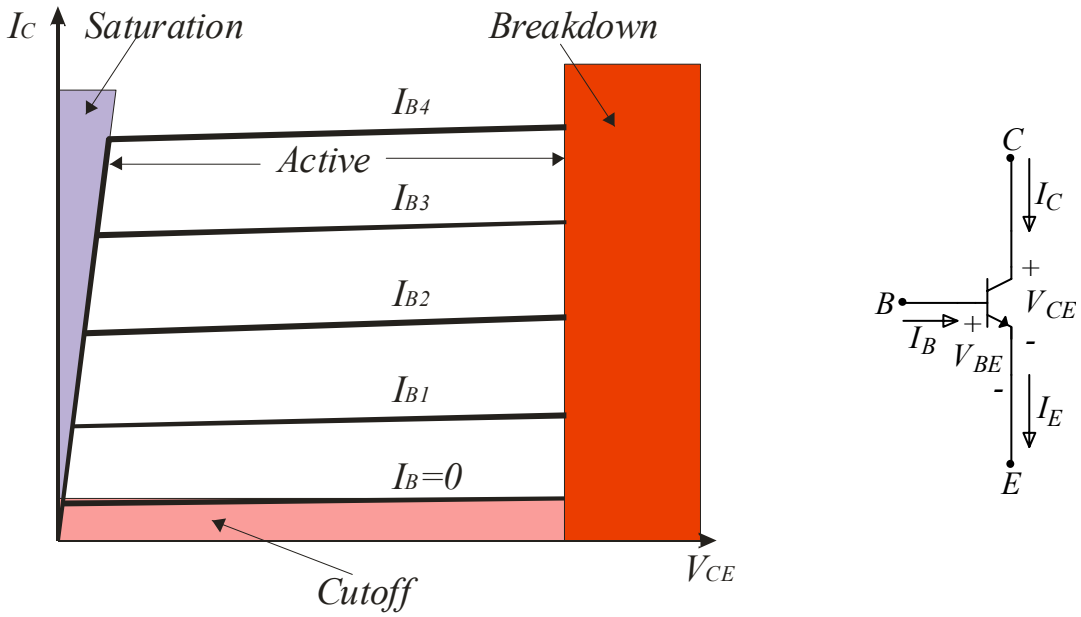


Figure 1. BJT characteristic curve

The characteristics of each region of operation are summarized below.

1. **cutoff region:**
   B-E junction is reverse biased. No current flow

2. **saturation region:**
   B-E and C-B junctions are forward biased
   Ic reaches a maximum which is independent of I_B and β.
   $V_{CE} < V_{BE}$. No control.

3. **active region:**
   B-E junction is forward biased, C-B junction is reverse biased
   $V_{BE} < V_{CE} < V_{CC}$, $I_C = \beta I_B$. Control

4. **breakdown region:**
   I_C and V_{CE} exceed specifications
   damage to the transistor

We will focus on operation in the active region. In this region of operation the model of the BJT is shown on Figure 2

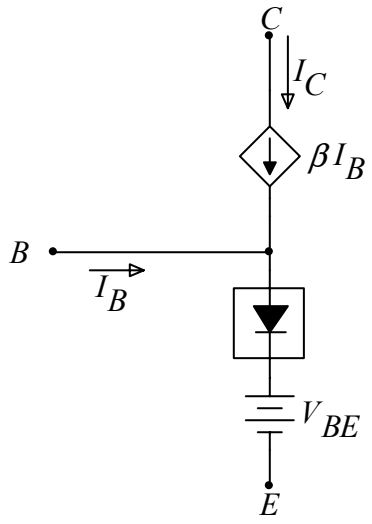


Figure 2. Large signal model of the BJT operating in the active region

The large signal model represents a simple state machine. The two states of interest are:

1. B-E junction is forward biased, $V_{BE} = 0.7$ Volts, current flows and the BJT is on
2. B-E junction is off, no current flows and the BJT is off.

We are interested in using the transistor as an amplifier with amplification A as shown on Figure 3 for which $V_0 = AV_I$

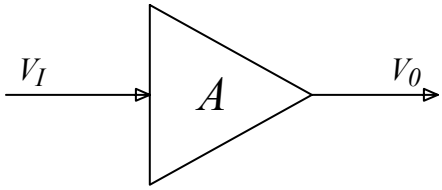


Figure 3. Amplifier symbol

For the generic BJT circuit the voltage transfer characteristic curve (output voltage versus input voltage) is shown on Figure 4. For amplification, the transistor must operate in the active or linear region.

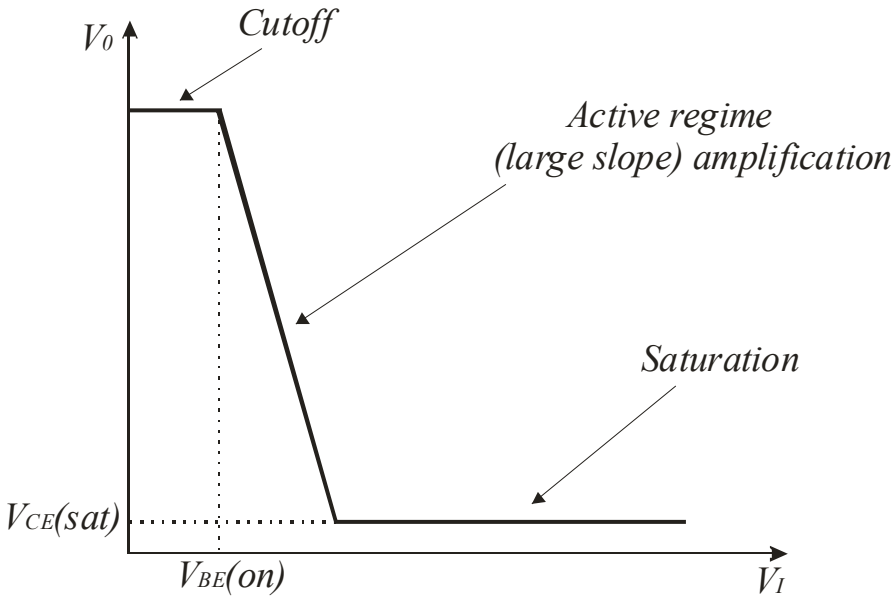


Figure 4. Voltage transfer curve for BJT circuit

This presents a challenge since we normally have a signal that is carried by, for example, a time dependent voltage which is permitted to go to (or through) zero. Now we can not simply apply this voltage to the base since the transistor would be moving in and out of the linear operation region.

Consider the amplifier circuit of Figure 5. We will qualitatively investigate the voltage transfer characteristics of this circuit for two cases of the input signal V_I. These two cases are graphically illustrated on Figure 6 (a) and (b).

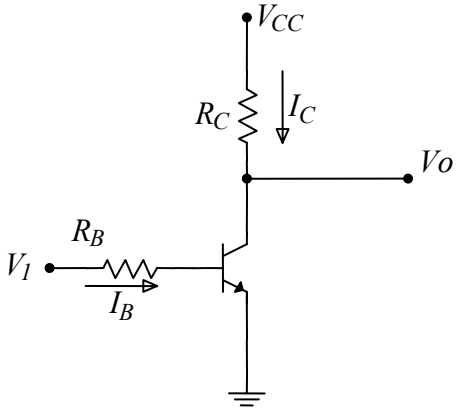
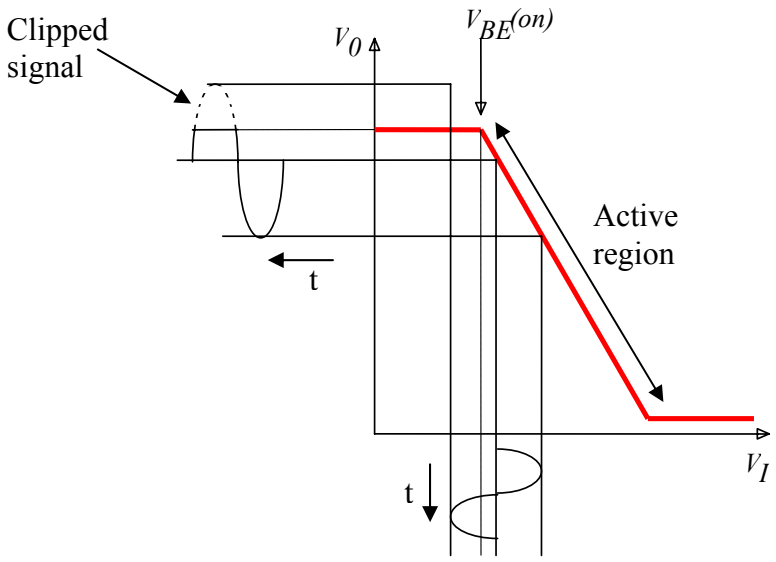


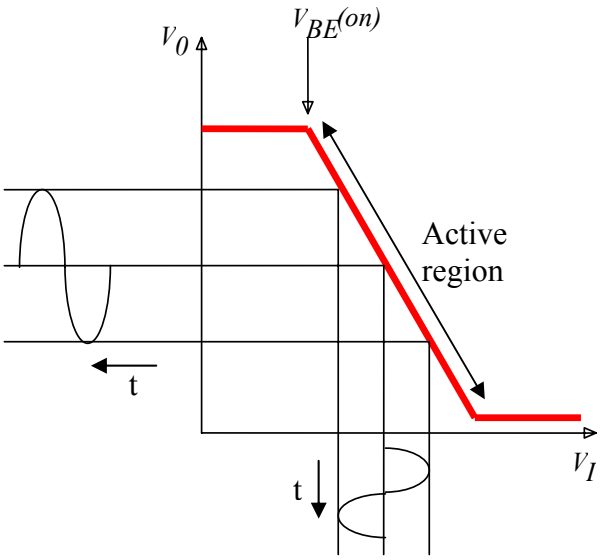
Figure 5. Amplifier circuit

The fluctuations of the input signal on Figure 6(a) result in excursions outside the active region of operation. As shown on the plot a portion of the signal is clipped. Compare this to the case shown on Figure 6 (b). Here the input signal has been shifted to the middle of the

active region and as a result the fluctuations of the input are within the range of operation and the complete amplified signal appears at the output.



(a)



(b)

Figure 6.

Therefore, the simple solution is to offset the input voltage to the middle of the linear response region. In this way the system may accept input voltage fluctuations and still

remain in the active region of operation. This offsetting of base voltage is called biasing and we will next investigate various circuit configurations that accomplish this task.

The Q-Point

The Quiescent Q-point corresponds to a specific point on the load line. The amplifier operates at the Q-point when the amplitude of the time varying signal is zero. This is shown on the characteristic curve shown on Figure 7.

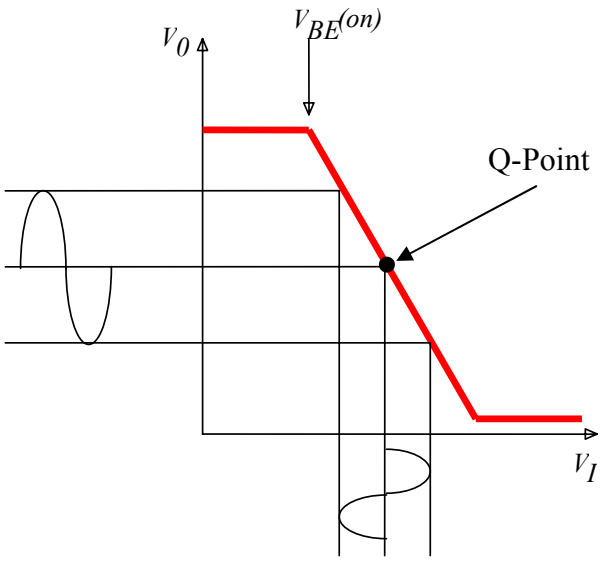


Figure 7

The Q-point may also be represented on the I_C versus V_{CE} characteristic plot as shown on Figure 8. Here the Q-point is at the intersection of the load line with one of the operating curves of the transistor.

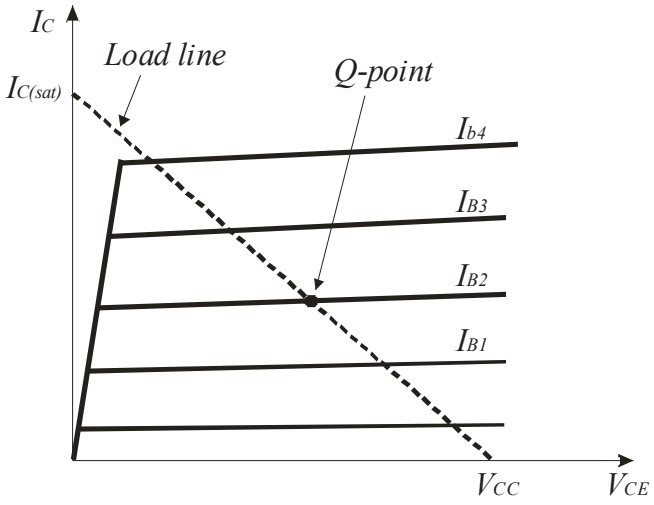


Figure 8

In fact the Q-point could be at any of the intersection points between the load line and the transistor curves. We have chosen the Q-point corresponding to I_{B2} on the plot of Figure 8 since that point is at about the midpoint of the load line. In amplifier design applications the Q-point corresponds to DC values for I_C and V_{CE} that are about half their maximum possible values as illustrated on Figure 9. This is called midpoint biasing and it represents the most efficient use of the amplifiers range for operation with AC signals. The range that the input signal can assume is the maximum and no clipping of the signal can occur (assuming that the signal range is less than the maximum available)

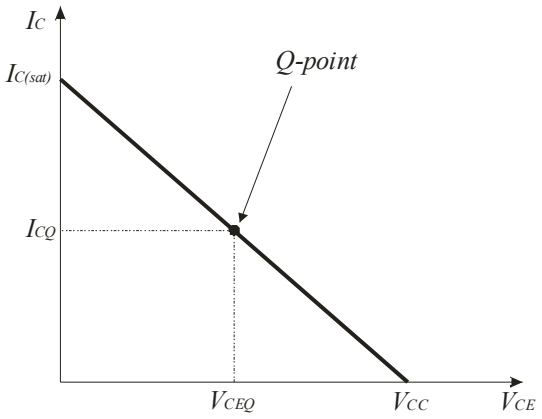


Figure 9. Q-point for midpoint biasing

BJT Bias Types

Base Bias.

Consider the circuit shown on Figure 10.

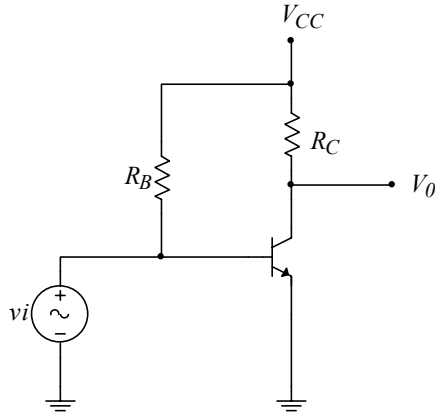


Figure 10. Base bias circuit

The DC operating point (Q-point) for this circuit is determined independent of the signal source *vi*. (We have indicated the AC signal by the lower case *v* in order to distinguish it from the DC operating point indicated by the capital *V*)

The DC current into the base may be determined by voltage around the base-emitter loop which gives

$$V_{CC} = I_B R_B + V_{BE} \tag{1.1}$$

and the DC base current becomes

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{1.2}$$

For operation in the active region,

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B} \tag{1.3}$$

Consideration of the collector-emitter loop gives

$$V_{CC} = I_C R_C + V_{CE} \tag{1.4}$$

And the collector current is

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{1.5}$$

Equation (1.5) is the load line equation for this circuit and it along with Equation (1.3) define the Q point.

We see that the Q-point for the Base-bias configuration depends on the β value of the transistor. The β value is an imprecise quantity and it is also a quantity whose value changes with temperature. Therefore, the Q-point will shift around as β changes which is not a desirable characteristic of the design.

DO NOT DESIGN WITH β

Voltage Divider Bias.

Next let's consider the circuit shown on Figure 11. Here we have used a voltage divider network at the base of the transistor and we have also added resistor R_E at the emitter. The capacitor C is called the coupling capacitor and it provides DC isolation between the amplifier and the signal source *vi*. Therefore the role of the coupling capacitor is to suppress all DC components that might be present in the signal *vi*.

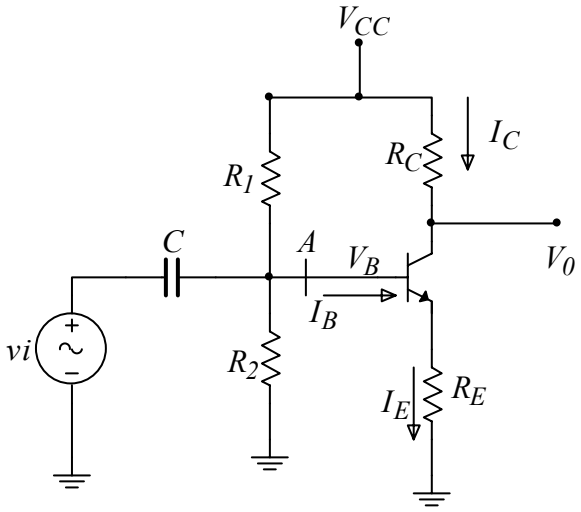


Figure 11. Voltage divider bias circuit

Now we need to take care of the biasing (i.e. the generation of the desirable DC voltage component at the base of the transistor). The most general biasing is to assume that the input signal can be both positive and negative. So, for *vi*= 0, set the output voltage, $V_0 = V_{CC}/2$ (mid range).

To find the base voltage corresponding to this set point we need to focus on the currents in the circuit. Recall that the defining equation for the BJT operation is given in terms of currents $(I_C = \beta I_B)$.

If $V_0 = V_{CC}/2$ then the voltage drop across R_C must also be $V_{CC}/2$ and the quiescent current is

$$I_{CQ} = \frac{V_{CC}}{2R_C} \tag{1.6}$$

Now the design is nearly set. Given the collector current, and knowing that we are in the linear region of operation, the base current is given by

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{V_{CC}}{2\beta R_C} \tag{1.7}$$

In DC, the Thevenin equivalent circuit to the left of point *A* is represented by the equivalent circuit shown on Figure 12 for which

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{1.8}$$

And

$$V_{TH} = V_{CC} \frac{R_2}{R_1 + R_2} \tag{1.9}$$

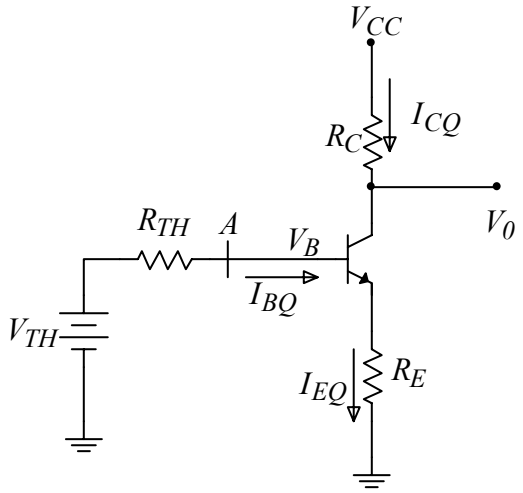


Figure 12

KVL around the base-emitter loop gives

$$V_{TH} = I_{BQ} R_{TH} + V_{BE(on)} + I_{EQ} R_E \tag{1.10}$$

Since the transistor is operating in the active region the emitter current is

$$I_{EQ} = (1+\beta) I_{BQ} \tag{1.11}$$

And so from Equation (1.10) the base current becomes

$$I_{BQ} = \frac{V_{TH} - V_{BE(on)}}{R_{TH} + (1+\beta)R_E} \tag{1.12}$$

And finally the quiescent collector current becomes

$$I_{CQ} = \beta I_{BQ} = \frac{\beta(V_{TH} - V_{BE(on)})}{R_{TH} + (1+\beta)R_E} \tag{1.13}$$

Our goal is to design a stable quiescent point. This is equivalent to having the quiescent point be independent of the β παραμετερ.

From Equation (1.13) we see that if $R_{TH} << (1+\beta)R_E$ then

$$I_{CQ} \cong \frac{\beta(V_{TH} - V_{BE(on)})}{(1+\beta)R_E} \tag{1.14}$$

And for $\beta >> 1$

$$I_{CQ} \cong \frac{V_{TH} - V_{BE(on)}}{R_E} \tag{1.15}$$

In practice making R_{TH} small is limited by power dissipation in resistors R_1 and R_2.
A general acceptable **design rule** is to have

$$\boxed{R_{TH} = \frac{1}{10}(1+\beta)R_E} \tag{1.16}$$

The quiescent collector-emitter voltage V_{CE} is found from the load line equation which is obtained by considering the C-E loop

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_{CQ}R_C - I_{EQ}R_E \\ &= V_{CC} - I_{CQ}R_C - \frac{1+\beta}{\beta} I_{CQ}R_E \\ &= V_{CC} - I_{CQ}\left(R_C + \frac{1+\beta}{\beta} R_E \right) \end{aligned} \tag{1.17}$$

Which for $\beta >> 1$ becomes

$$V_{CEQ} \cong V_{CC} - I_{CQ}\left(R_C + R_E \right) \tag{1.18}$$

The Q-point is thus defined by Equations (1.15) and (1.18).

We have thus derived the conditions for obtaining a stable Q-point (no β dependence) using the voltage divider bias.

Equation (1.18) also shows that the effective load resistance seen by the DC collector circuit is $R_C + R_E$

Now let's consider the small signal gain of the amplifier.

Recall that the transistor operates in the active (linear) region and at the Q-point, the B-E loop and the C-E loop give respectively

$$V_{TH} = I_{BQ}R_{TH} + V_{BE(on)} + I_{EQ}R_E \tag{1.19}$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E \tag{1.20}$$

If a small signal *vi* is superimposed on the input of the circuit shown on Figure 12 the corresponding circuit is shown on Figure 13.

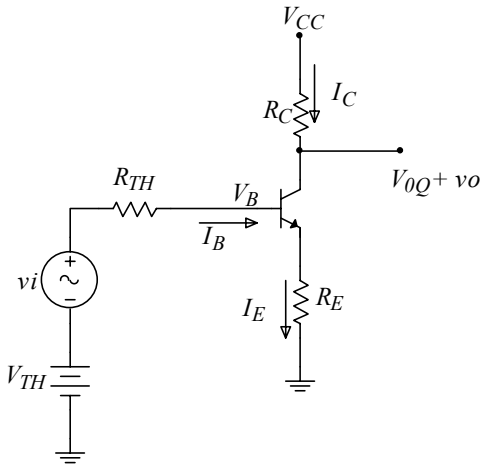


Figure 13

The output signal is now a superposition of the Q-point and the signal *vi*.

Therefore the B-E loop KVL gives

$$vi = i_b R_{TH} + v_{be} + i_e R_E \tag{1.21}$$

And the C-E loop gives

$$i_b R_C + v_{ce} + i_e R_E = 0 \tag{1.22}$$

Where the parameters i_e, i_b, v_{ce} are due to the small signal and $v_{be} = 0$ since the transistor is already on and the junction voltage is constant.

The voltage gain of the device is the ratio

$$\frac{v_o}{vi} = -\frac{\beta i_b R_C}{(\beta+1) i_b R_E + i_b R_{TH}} = -\frac{\beta R_C}{(\beta+1) R_E + R_{TH}} \tag{1.23}$$

Recall that for Q-point stability we have constrained $R_{TH} << (1+\beta) R_E$ and thus for large β the gain reduces to

$$\boxed{\frac{v_o}{vi} \cong -\frac{R_C}{R_E}} \tag{1.24}$$

So the device has a constant gain and it is an inverter.

A question arises naturally by observing the gain Equation (1.24): What happens when R_E becomes zero. Before making any conclusions on the value of the gain we must consider the details of the base-emitter junction. This is a diode junction and it has an effective resistance given by

$$r_{BE} = \frac{\frac{kT}{q}}{i_E} \tag{1.27}$$

The temperature dependence of this resistance makes it a very poor parameter to fely upon on a design (unless we desire to measure temperature by exploiting this dependence).

Therefore we normally require an emitter resistor $R_E > r_E$.