6.012 - Microelectronic Devices and Circuits

Lecture 20 - Diff-Amp Anal. I: Metrics, Max. Gain - Outline

- **Announcements**
  - **Announcements - D.P.:** No Early effect in large signal analysis; just LECs. Lec. 21 foils useful; Sp 06 DP foils, too (on Stellar)
  - **Do PS #10:** free points while working on D.P.
- **Review - Differential Amplifier Basics**
  - **Difference- and common-mode signals:** $v_{ID}=v_{IN1}-v_{IN2}$, $v_{IC}=(v_{IN1}+v_{IN2})/2$
  - **Half-circuits:** half of original with wires shorted or cut **(familiar, easy analyses)**
- **Performance metrics - specific to diff. amps.**
  - **Difference- and common-mode gains**
  - **Common-mode rejection ratio**
  - **Input and output voltage swings**
- **Non-linear loads**
  - **The limitation of resistive loads:** Gain limited by voltage supply
  - **Non-linear loads:** High incremental resistance/small voltage drop
- **Active loads**
  - **Lee load**
  - **Current mirror load**

Differential Amplifiers - overview of features and properties

Intrinsic advantages and features:

- large difference mode gain
- small common mode gain
- easy to cascade stages; no coupling capacitors
- no emitter/source capacitors in CS/CE stages

Performance metrics:

- difference mode voltage gain, A_{vd}	Today
- common mode voltage gain, A_{vc}	Today
- input resistance, R_{in}	∞
- output resistance, R_{out}	Lec 21
- common mode input voltage range	Today
- output voltage swing	Today
- DC offset on output	Lec 21
- Power dissipation	Lec 18

Differential Amplifiers - common-mode input range

$(V_{C,min} \le v_C \le V_{C,max})$

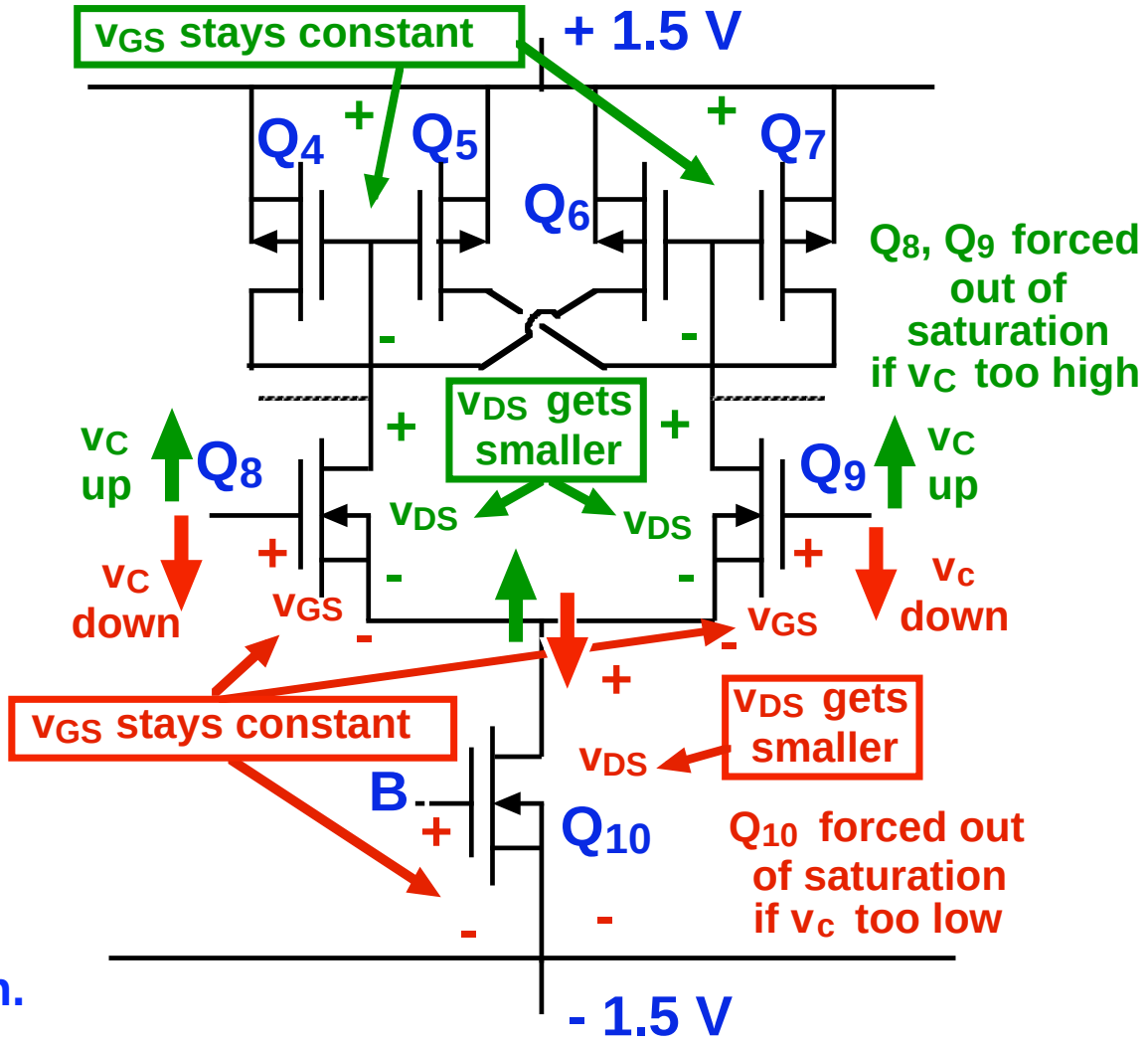
We have said the output changes very little for common-mode inputs.

This is true as long as the v_C doesn't push the transistors out of saturation.

There are a minimum and maxiumum v_C:

$V_{C,max}$: As v_C increases, v_{DS8} and v_{DS9} decrease until Q_8 and Q_9 are no longer in saturation.

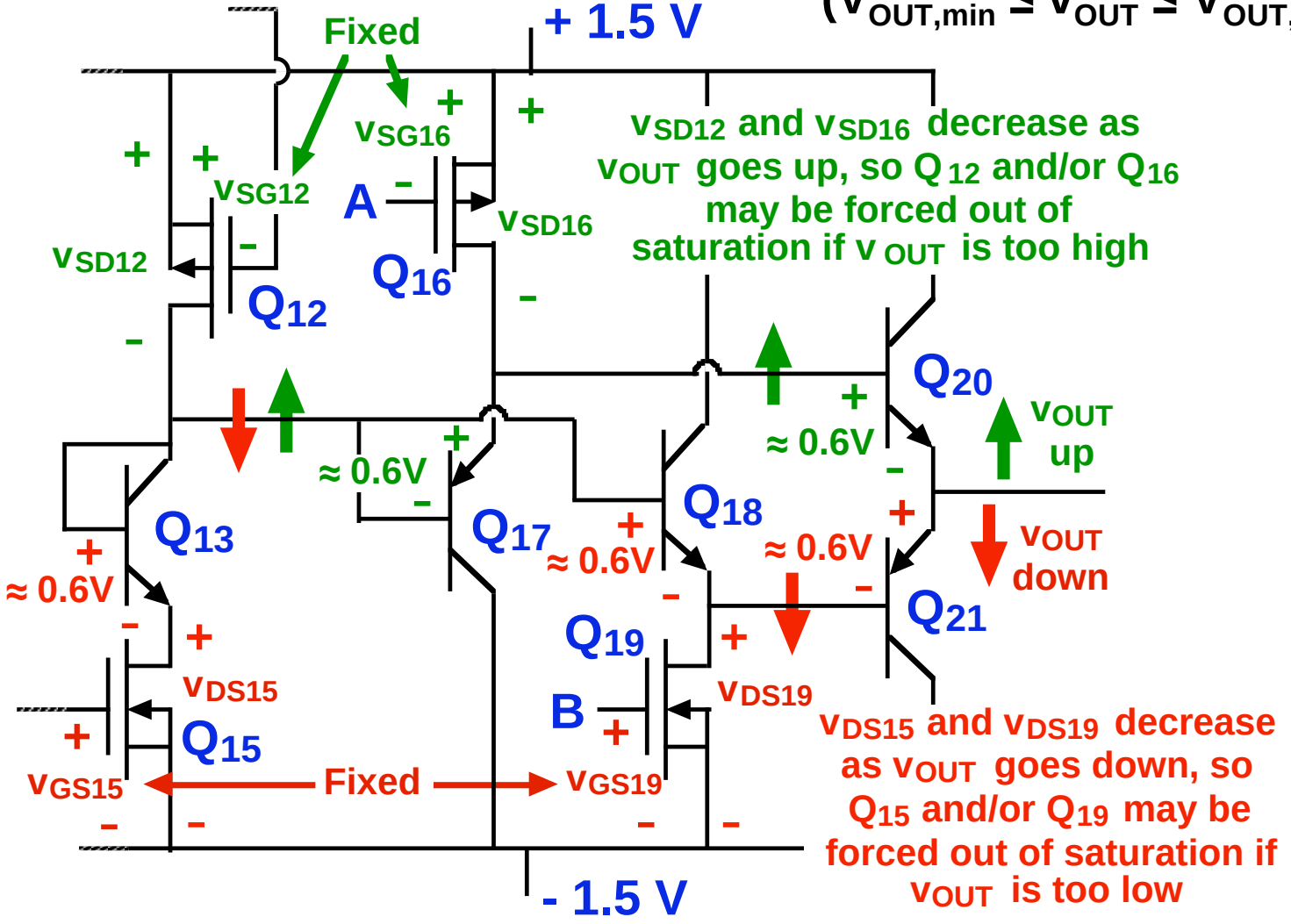
$V_{C,min}$: As v_C decreases, v_{DS10} decreases until Q_{10} is no longer in saturation.



The node between Q_8/Q_9 and Q_{10} moves up and down with v_C.

Differential Amplifiers - output voltage range

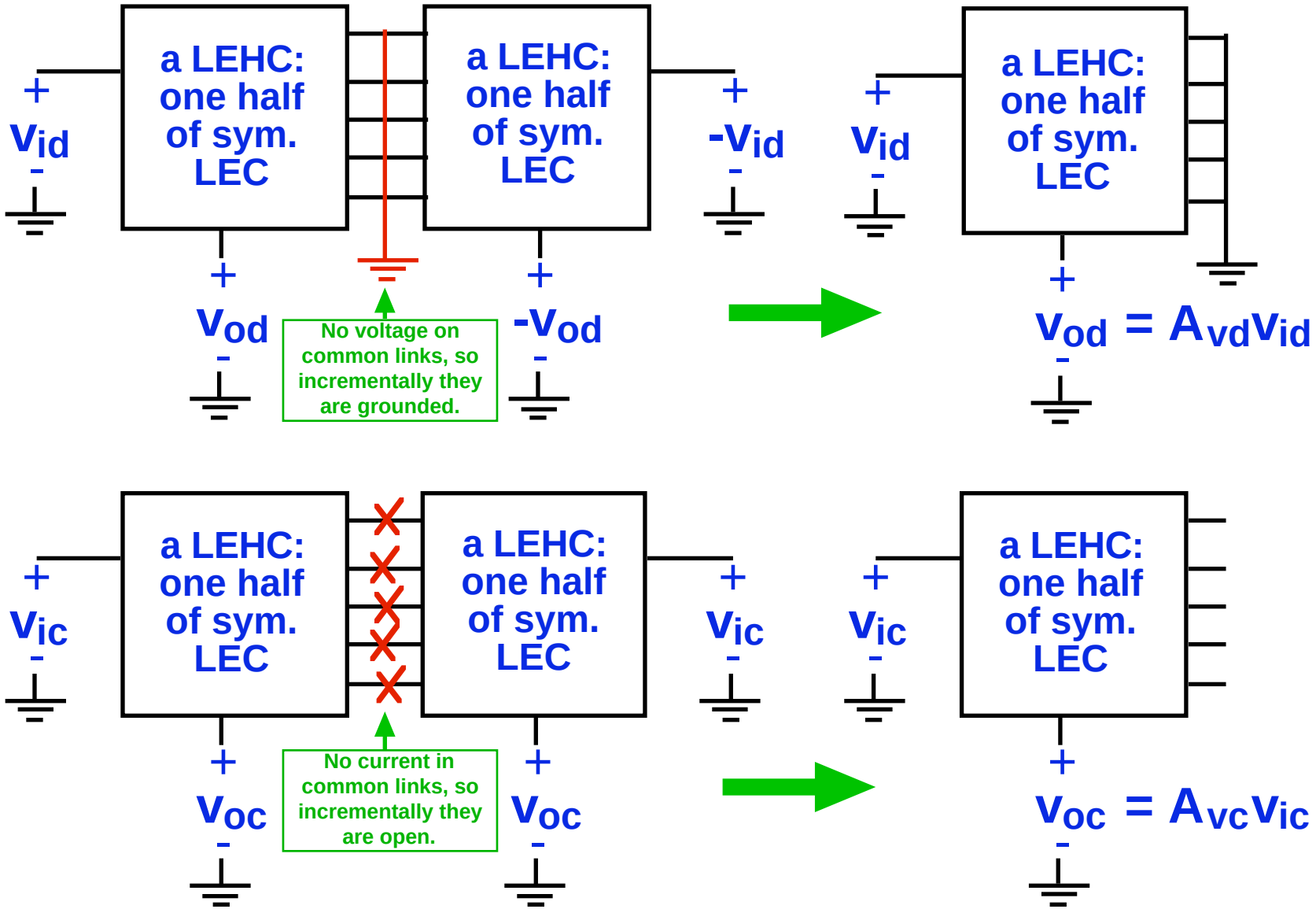
$(V_{OUT,min} \le v_{OUT} \le V_{OUT,max})$



As v_{OUT} goes down, Q_{15} and/or Q_{19} may go out of saturation; as v_{OUT} goes up, the same may happen to Q_{12} and/or Q_{16}.

Differential Amplifier Analysis -

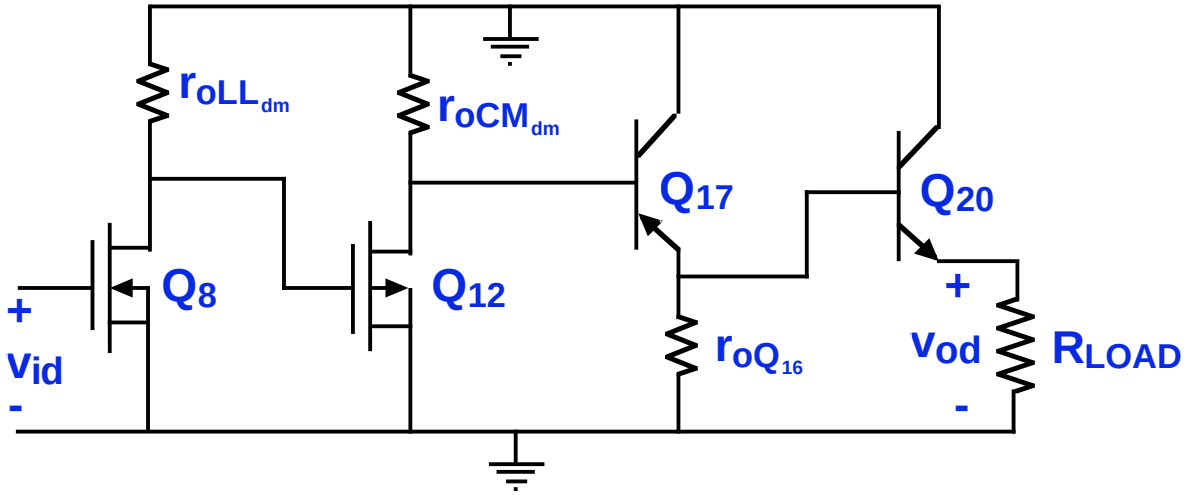
incremental analysis exploiting symmetry and superposition



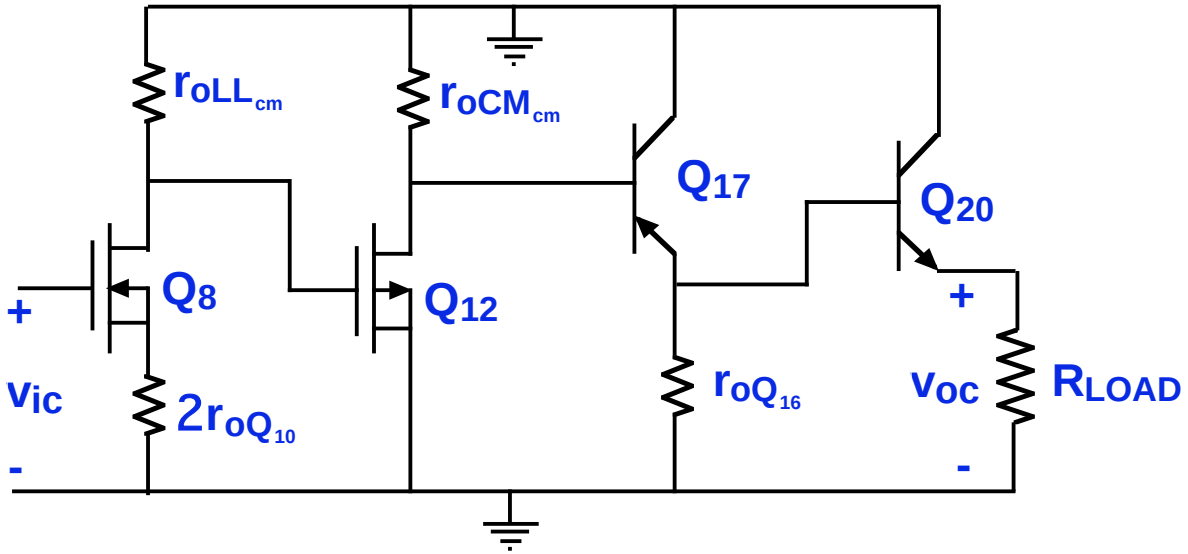
Looking at the design problem circuit:

Lesson - Draw the difference and common mode half circuits.

Difference mode half circuit:



Common mode half circuit:



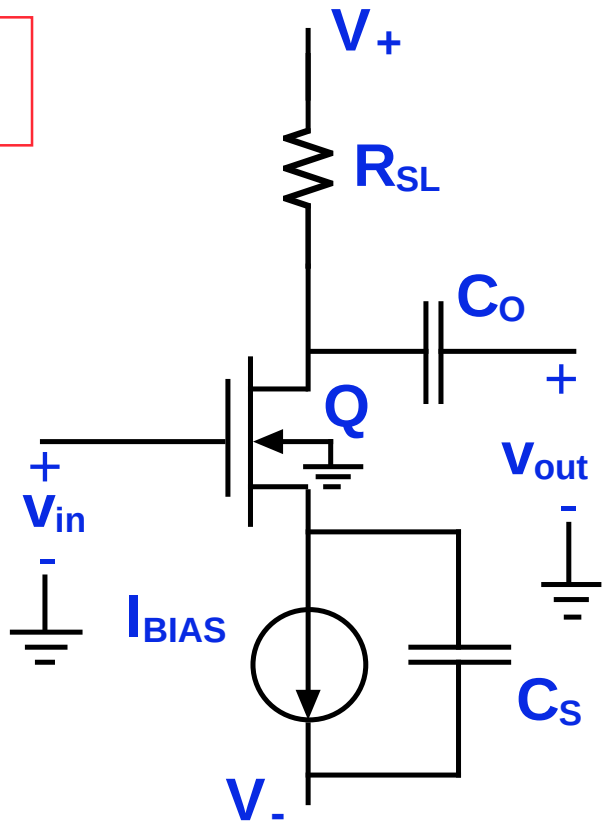
We have reduced the transistor count from 22 to 4, and we see that our complex amplifier is a just cascade of 4 single-transistor stages.

What's with these active, nonlinear loads?
Why doesn't the design problem use resistors?

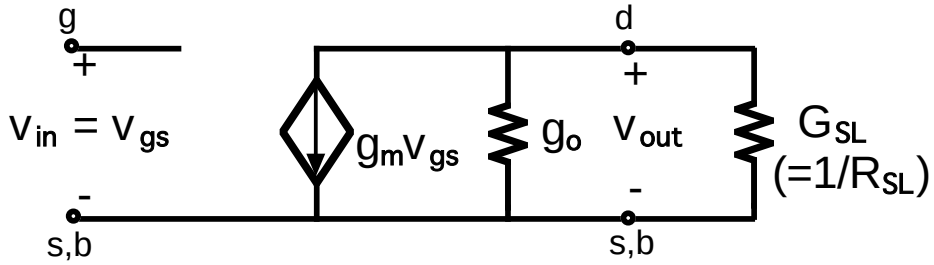
Linear Resistor Loads:

the limit on maximum stage gain

- **with linear resistor loads we must make a compromise between the voltage gain and the size of the output voltage swing.**



Maximum voltage gains



$$\text{MOSFET}^{*}: \quad \left|A_{v,\max}\right| = g_m R_{SL} = \frac{2 I_D R_{SL}}{\left[V_{GS} - V_T\right]} \le \frac{2\left[I_D R_{SL}\right]_{\max}}{\left[V_{GS} - V_T\right]_{\min}}$$

$$\text{Bipolar}: \quad \left|A_{v,\max}\right| = g_m R_{SL} = \frac{q I_C R_{SL}}{kT} \le \frac{\left[I_C R_{SL}\right]_{\max}}{V_{Thermal}}$$

What are $[I_C R_{SL}]_{max}$, $[I_D R_{SL}]_{max}$, and $[V_{GS} - V_T]_{min}$?

* For a MOSFET, $g_m = (2KI_D/\alpha)^{1/2} = K(V_{GS} - V_T)/\alpha = 2I_D/(V_{GS} - V_T)$

Resistor Loads: cont.

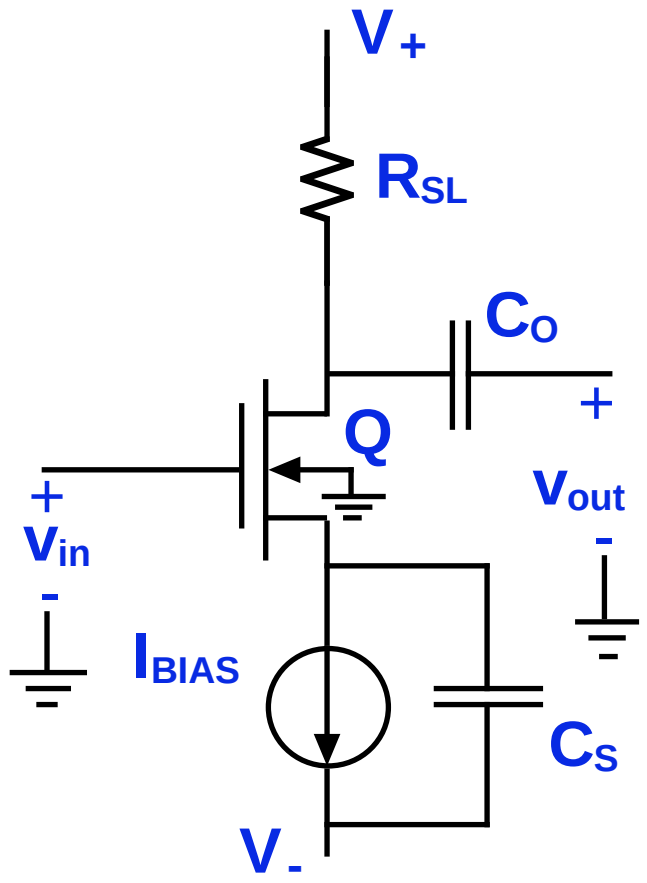
- What are $[I_D R_{SL}]_{max}$, $[I_C R_{SL}]_{max}$, and $[V_{GS} - V_T]_{min}$?

$[I_D R_{SL}]_{max}$, $[I_C R_{SL}]_{max}$:

- $[I_D R_{SL}]_{max}$ and $[I_C R_{SL}]_{max}$ are determined by the desired voltage swing at the output and/or by the common-mode input voltage range.
- The ultimate limit is the power supply.

$[V_{GS} - V_T]_{min}$:

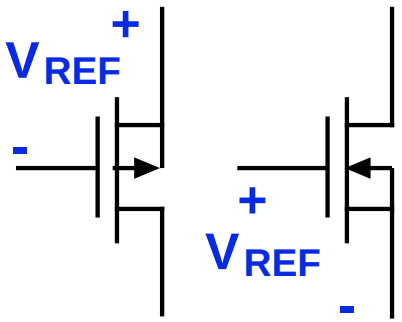
- $[V_{GS} - V_T]_{min}$ is set by how close to threshold the gate can safely be biased before the strong inversion, drift model fails. We will say more about this shortly (Slide 23).

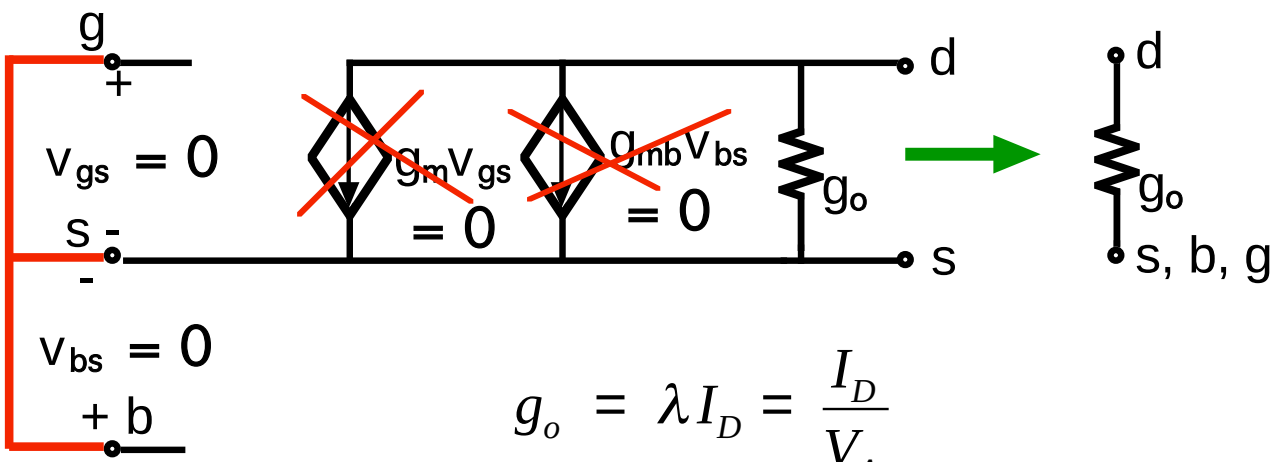


Current Source Loads: Incrementally large resistance
Relatively small quiescent voltage drop

- transistors with a DC input voltage, i.e. set up as sources/sinks -

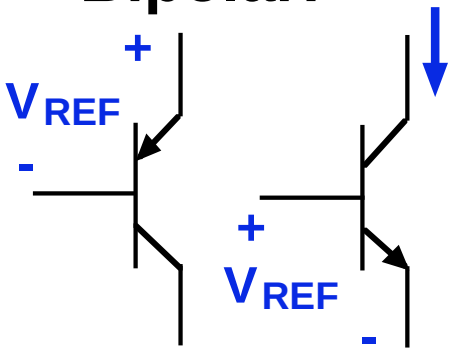
MOSFET:

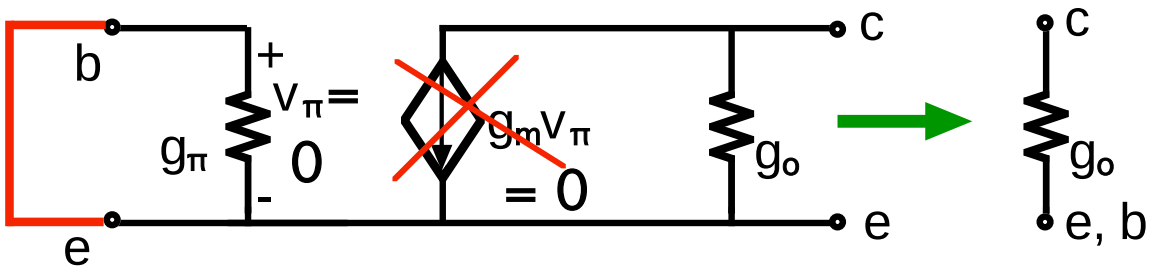




$$g_o = \lambda I_D = \frac{I_D}{V_A}$$

Bipolar:



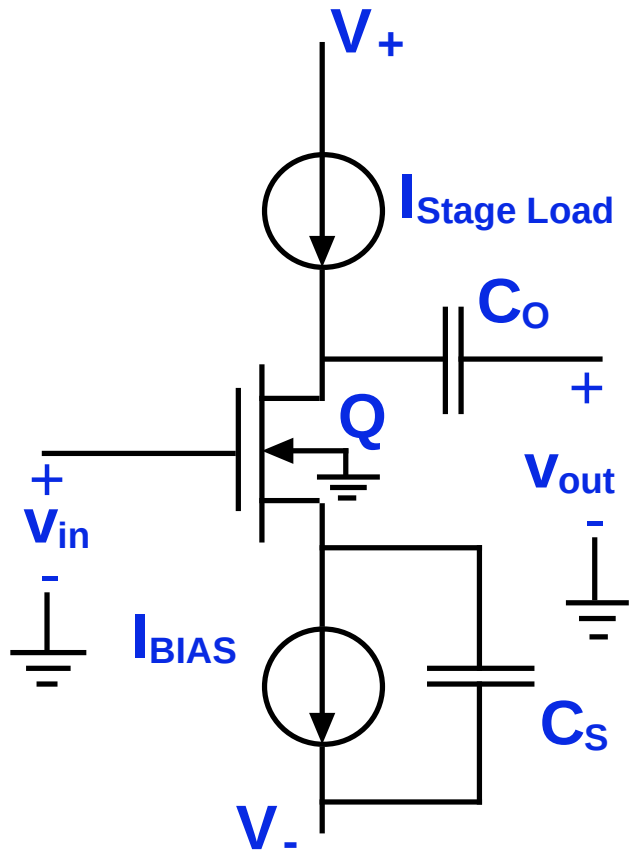


$$g_o = \lambda I_C = \frac{I_C}{V_A}$$

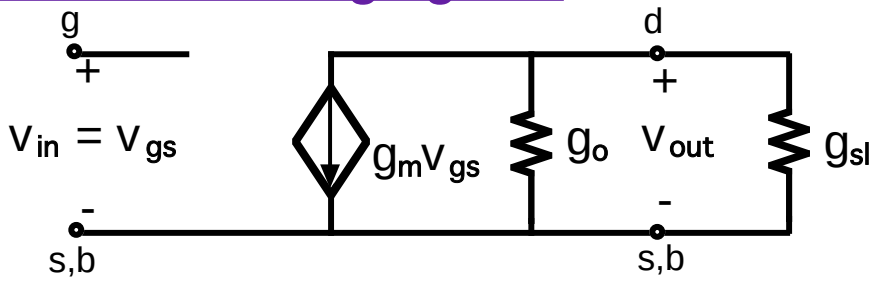
Current Source Loads:

the limit on the maximum stage gain

- **current source loads eliminate the need to compromise between the voltage gain and the output voltage swing**



Maximum voltage gains



$$\text{MOSFET}^{*}: \quad |A_{v,\max}| = \frac{g_m}{g_o + g_{sl}} = \frac{2I_D/[V_{GS} - V_T]}{I_D/V_{A,Q} + I_D/V_{A,SL}} \le \frac{2V_{A,eff}}{[V_{GS} - V_T]_{\min}}$$

$$\text{Bipolar}: \quad |A_{v,\max}| = \frac{g_m}{g_o + g_{sl}} = \frac{qI_C/kT}{I_C/V_{A,Q} + I_C/V_{A,SL}} = \frac{V_{A,eff}}{V_t}$$

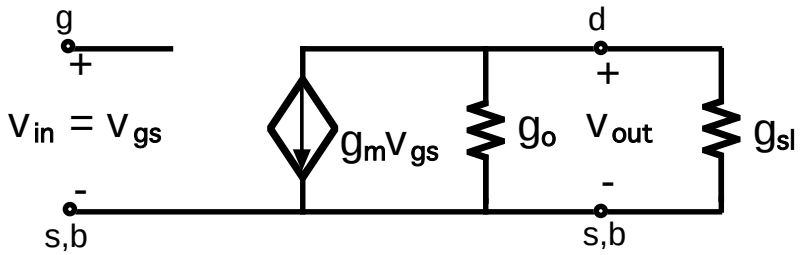
$$\text{with} \quad V_{A,eff} \equiv \frac{V_{A,Q}V_{A,SL}}{[V_{A,Q} + V_{A,SL}]}, \quad V_t \equiv \frac{kT}{q}$$

Typically $V_{A,eff}$ >> $[I_D R_{SL}]_{max}$

*** For a MOSFET, $g_m = (2KI_D/\alpha)^{1/2} = K(V_{GS} - V_T)/\alpha = 2I_D/(V_{GS} - V_T)$**

Current Source Loads: the maximum stage gain, cont.

- the similarity in the results for BJT's and MOSFETs operating in strong inversion extends to MOSFETs operating sub-threshold and in velocity saturation, also:



The MOSFET LEC: the same for all.

Maximum voltage gains

MOSFET sub-threshold: $i_D = I_{S,s-t} e^{(v_{GS}-V_T)/nV_t}, \quad g_m = \dfrac{I_D}{nV_t}$

$$\left|A_{v,\max}\right| = \frac{g_m}{g_o + g_{sl}} = \frac{I_D/nV_t}{I_D/V_{A,Q} + I_D/V_{A,SL}} = \frac{V_{A,eff}}{nV_t}$$

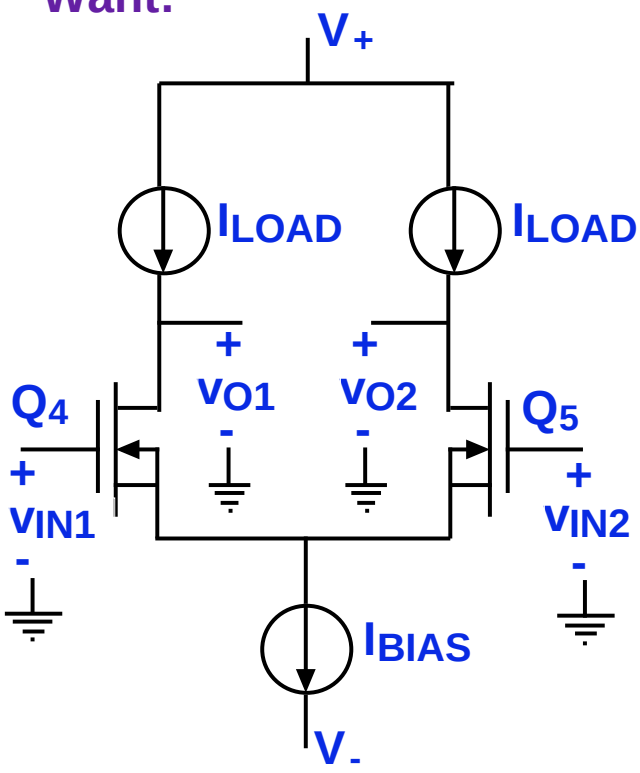
MOSFET w. velocity saturation: $i_D = W\, s_{sat}\, C^*_{ox}\left(v_{GS} - V_T\right), \quad g_m = W\, s_{sat}\, C^*_{ox} = \dfrac{I_D}{\left(v_{GS} - V_T\right)}$

$$\left|A_{v,\max}\right| = \frac{g_m}{g_o + g_{sl}} = \frac{I_D/\left(v_{GS} - V_T\right)}{I_D/V_{A,Q} + I_D/V_{A,SL}} \le \frac{V_{A,eff}}{\left(v_{GS} - V_T\right)_{\min}}$$

with $V_{A,eff} \equiv \dfrac{V_{A,Q} V_{A,SL}}{\left[V_{A,Q} + V_{A,SL}\right]}$

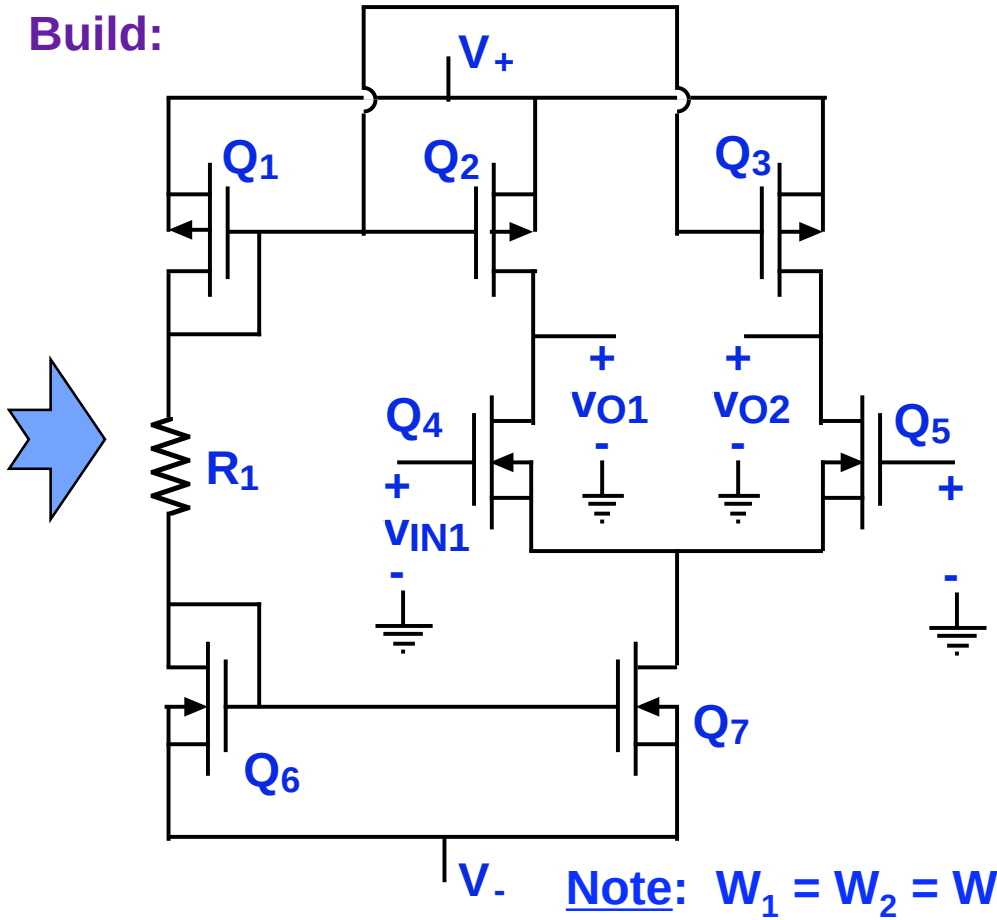
Current Source Loads: Example - biasing a source-coupled pair differential amplifer stage

Want:



Note: $I_{LOAD} = I_{BIAS}/2$

Build:

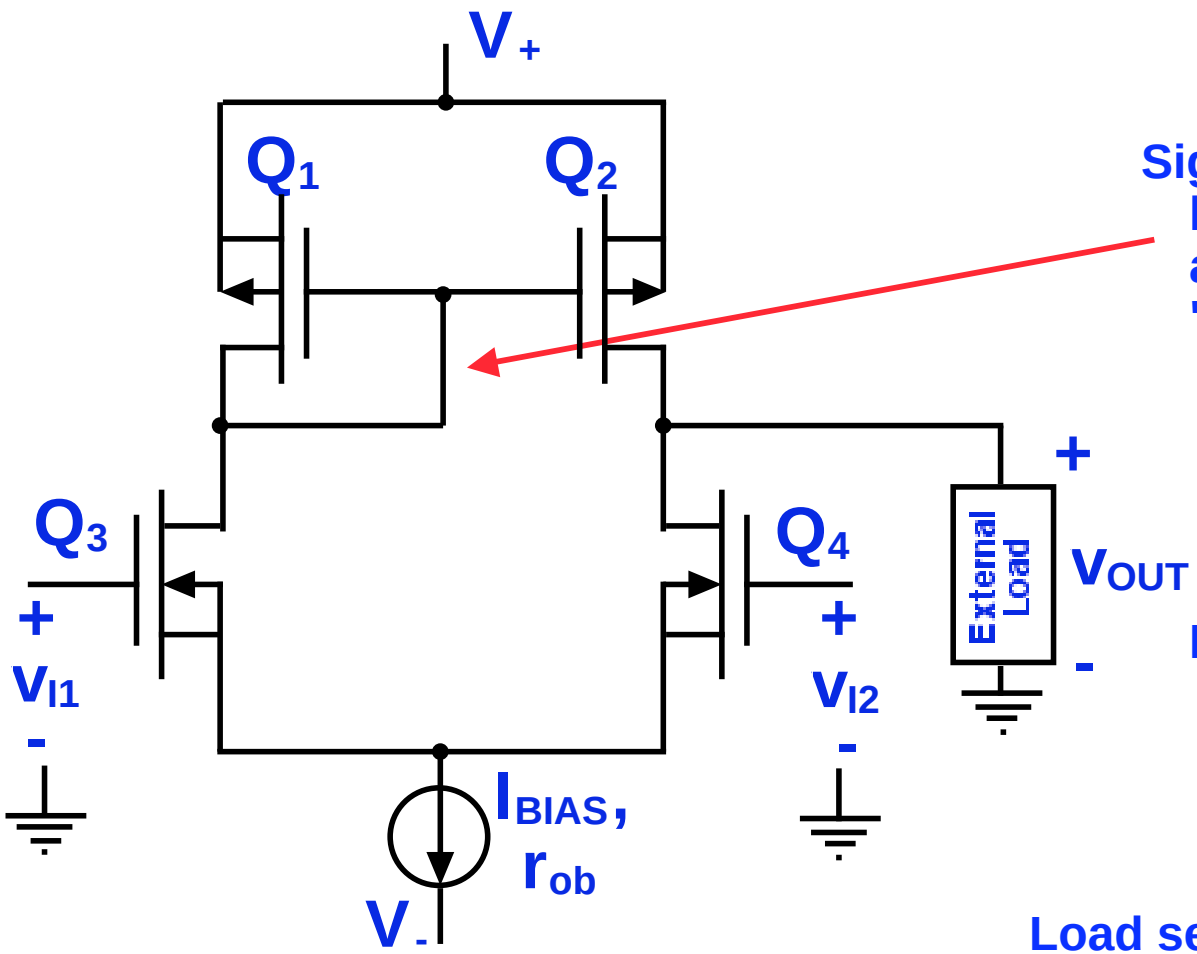


Note: $W_1 = W_2 = W_3$
$W_7 = 2W_6$

This is nice…can we do even better?
Yes, with active loads. Consider…

Active Loads:

Loads that don't just sit there and look pretty.
First example: the current mirror load



Signal actively fed from left side to right side, and applied inputs to "stage load" MOSFETs.

Now "single ended," i.e. only one output, but it is twice as large:

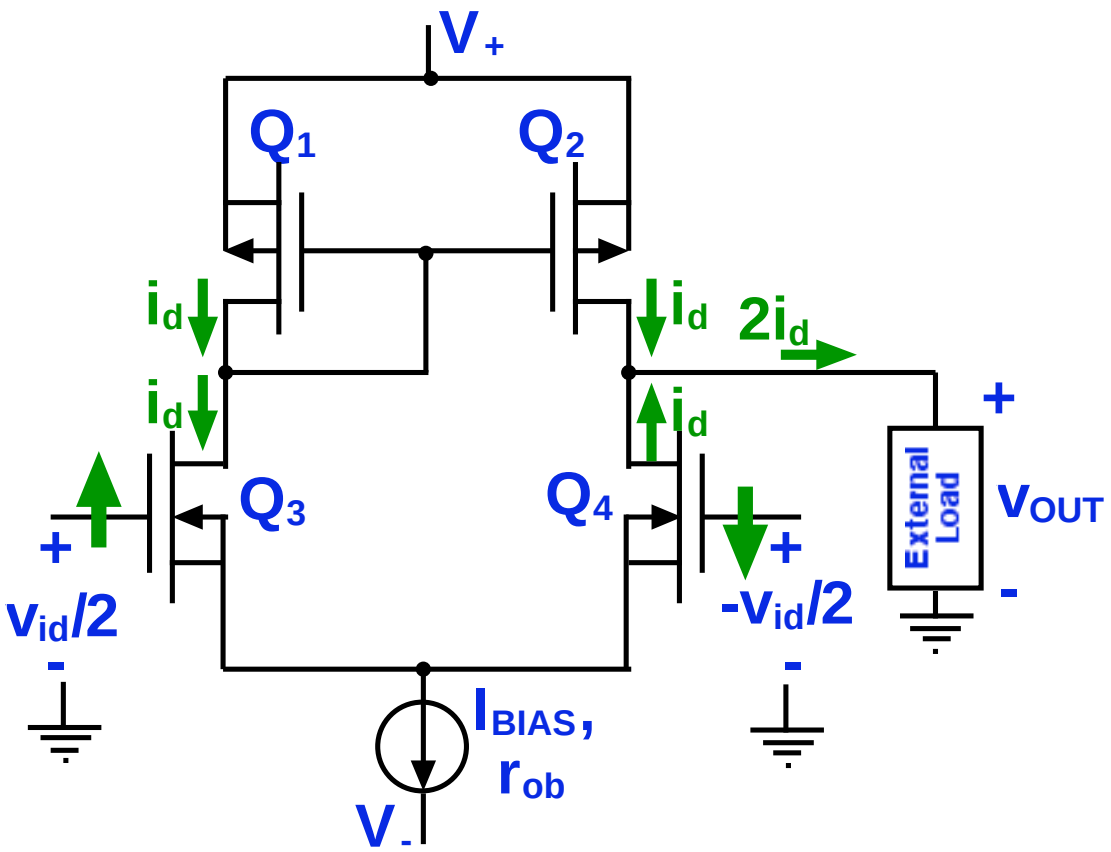
$v_{out} = 2v_{out1}$

Load self-adjusting; circuit forces $I_{LOAD} = I_{BIAS}/2$.

Active Loads: The current mirror load, cont.

Large differential-mode gain, small common-mode gain.
Also provides high gain conversion from double-ended to single-ended output.

The circuit is no longer symmetrical, so half-circuit techniques can not be applied. The full analysis is found in the course text. We find:



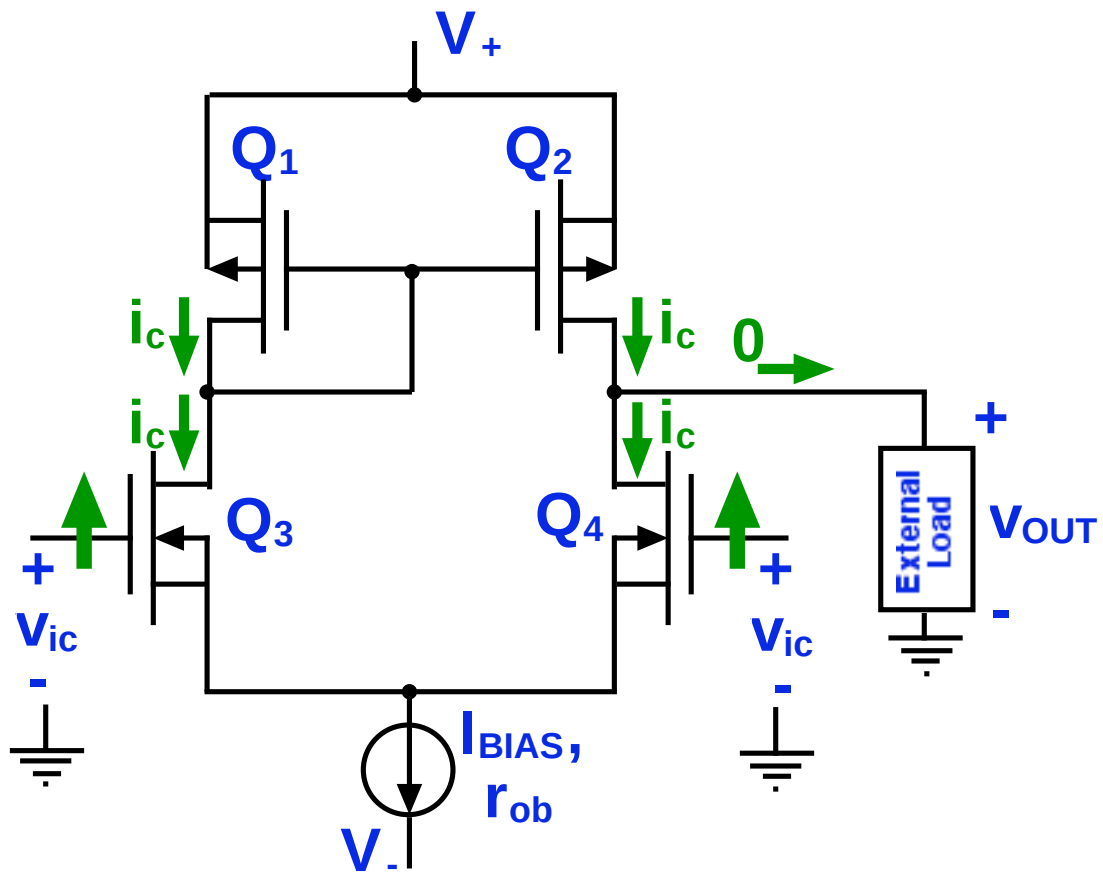
Difference-mode inputs

$$v_{out,d} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} v_{id}/2$$

Active Loads: The current mirror load

Common-mode inputs

$$v_{out,c} = \frac{g_{ob}}{2g_{m2}} v_{ic}$$



With both inputs:

$$v_{out} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{ob}}{2g_{m2}} \frac{(v_{in1} + v_{in2})}{2}$$

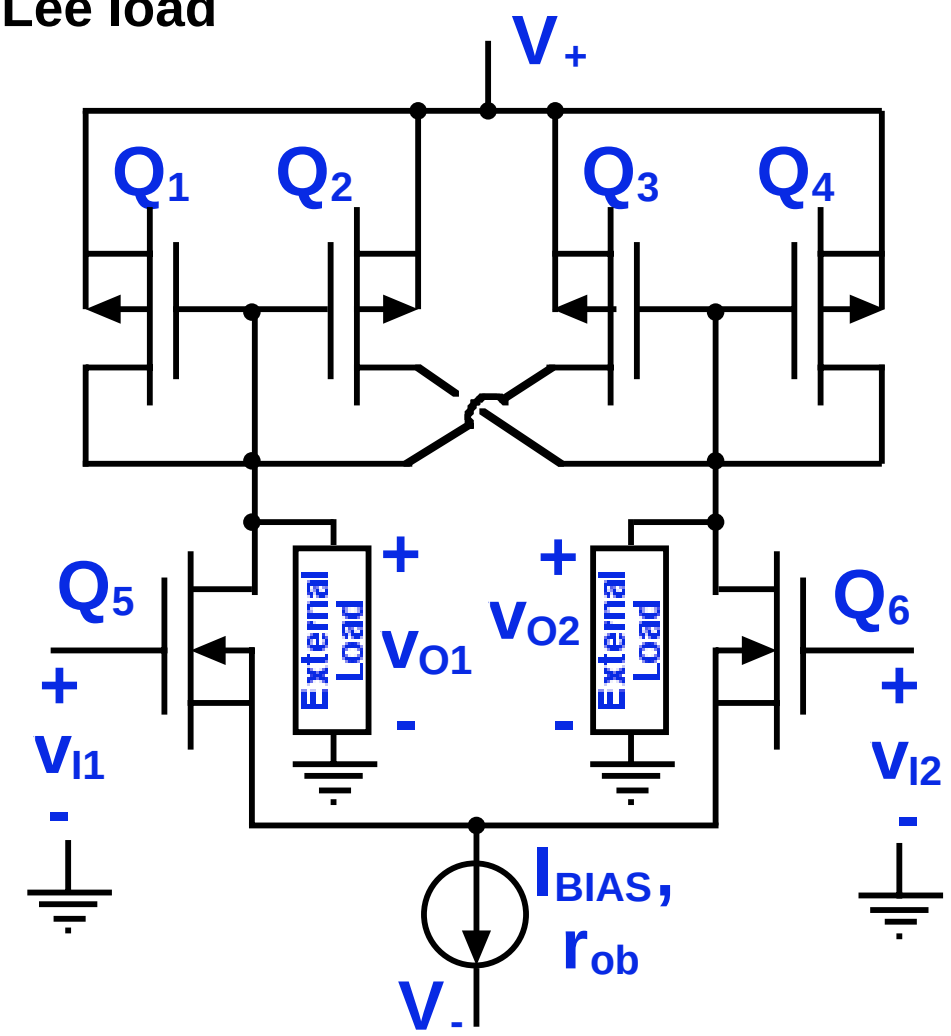
Note: In D.P. the output goes to the base of two BJTs; $g_{el} \neq 0$ and can be important.

What if we want an active load and yet stay differential?

Active Loads - The Lee load

A load for a fully-differential stage that looks like a large resistance in difference-mode and small resis-tance in common-mode)

The conventional schematic is drawn here, but the coup-ling of the load and what is happening is made clearer by redrawing the circuit (next slide.)

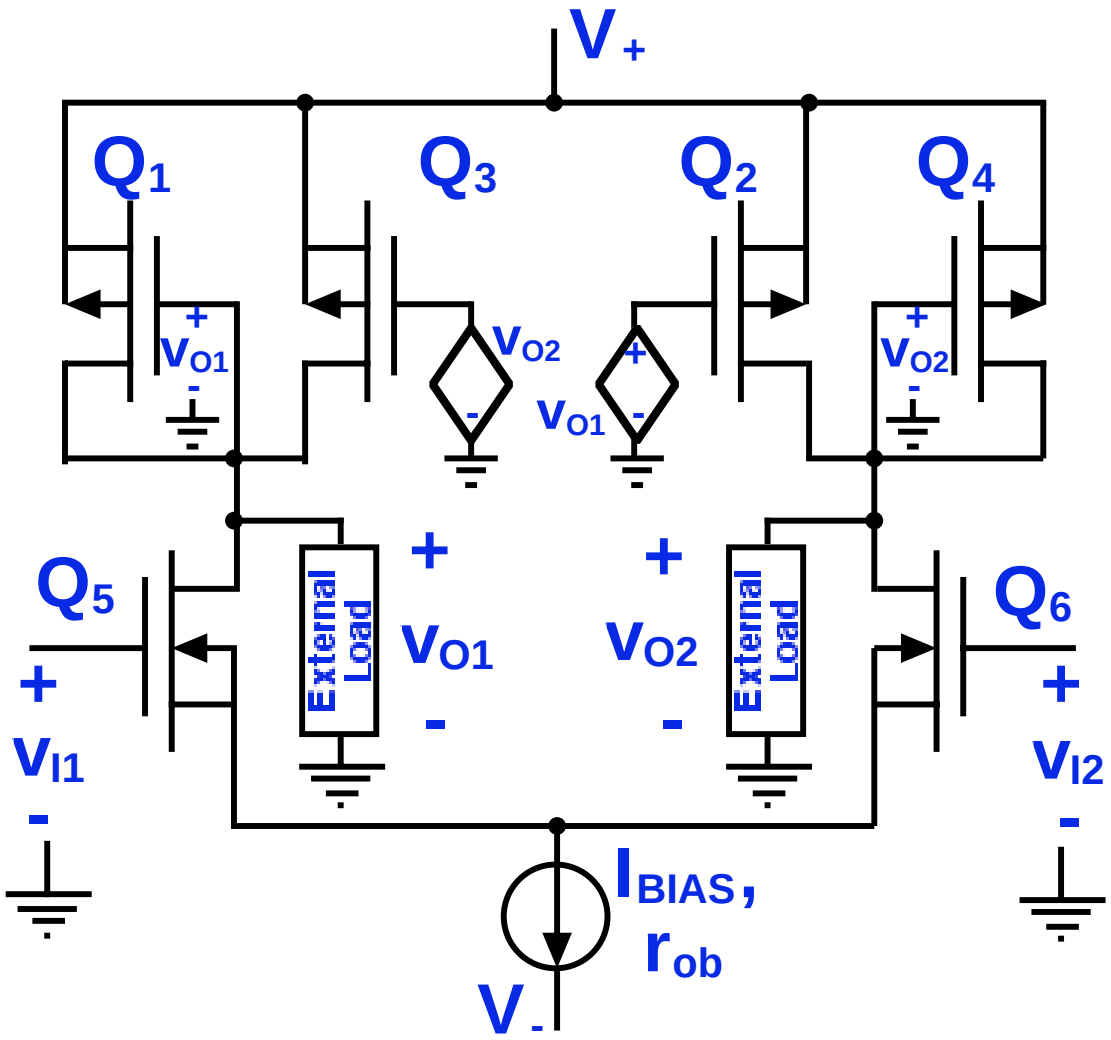


Normal format

Active Loads - The Lee load. cont.

Drawn as on the right we see that the load MOSFETs on each side are driven by both out-puts. The result is different if the two outputs are equal and opposite (diff-mode operation) or if they are equal (common-mode).

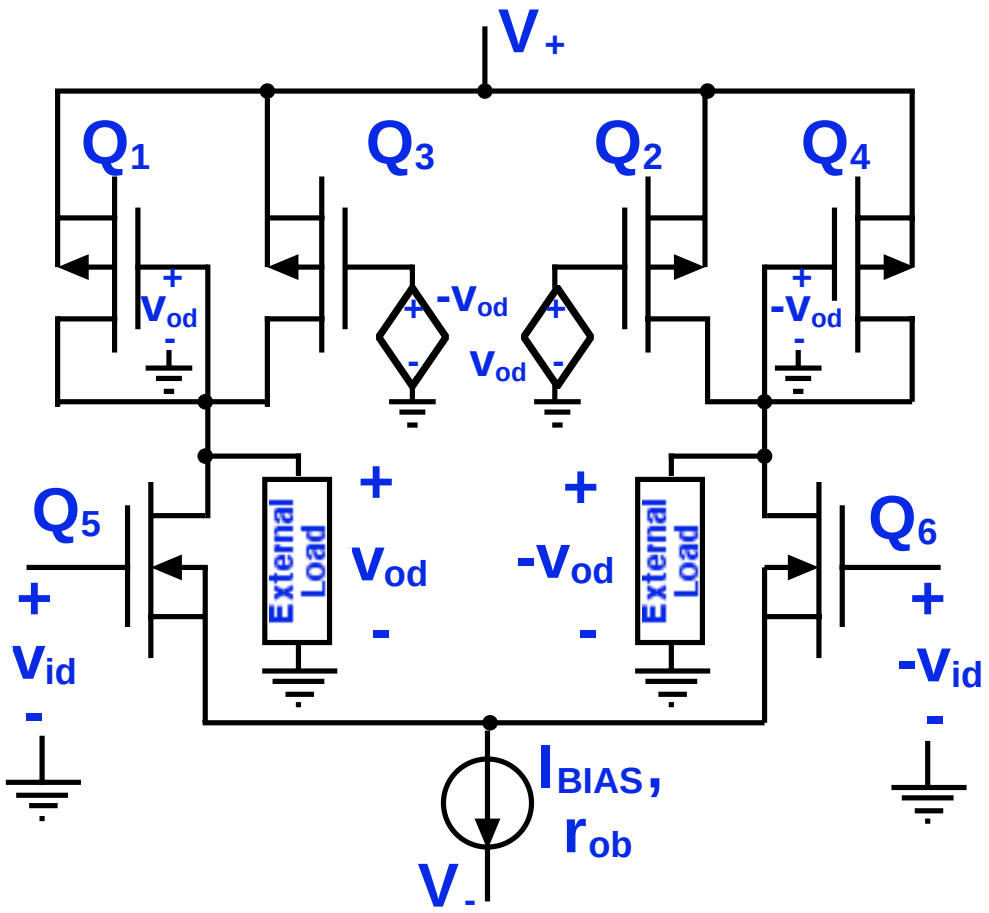
The next few slides give the results for each mode.



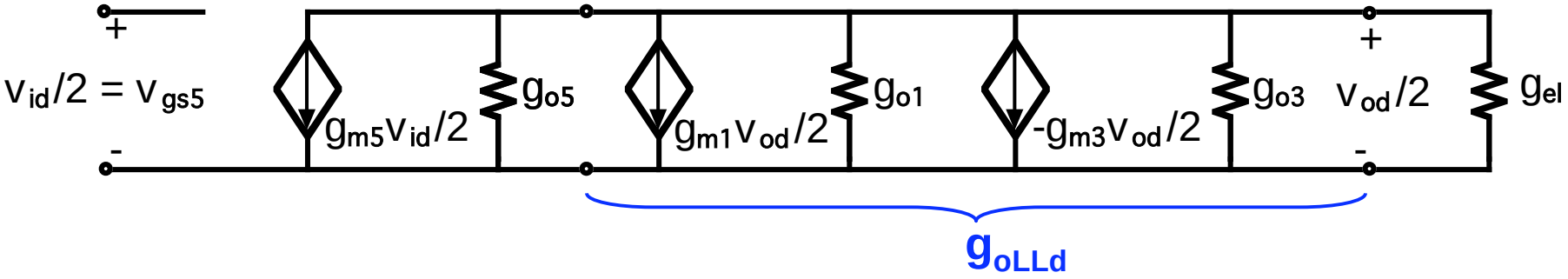
Drawn to highlight cross-coupling and demonstrate symmetry

The Lee load:

analysis for difference-mode inputs

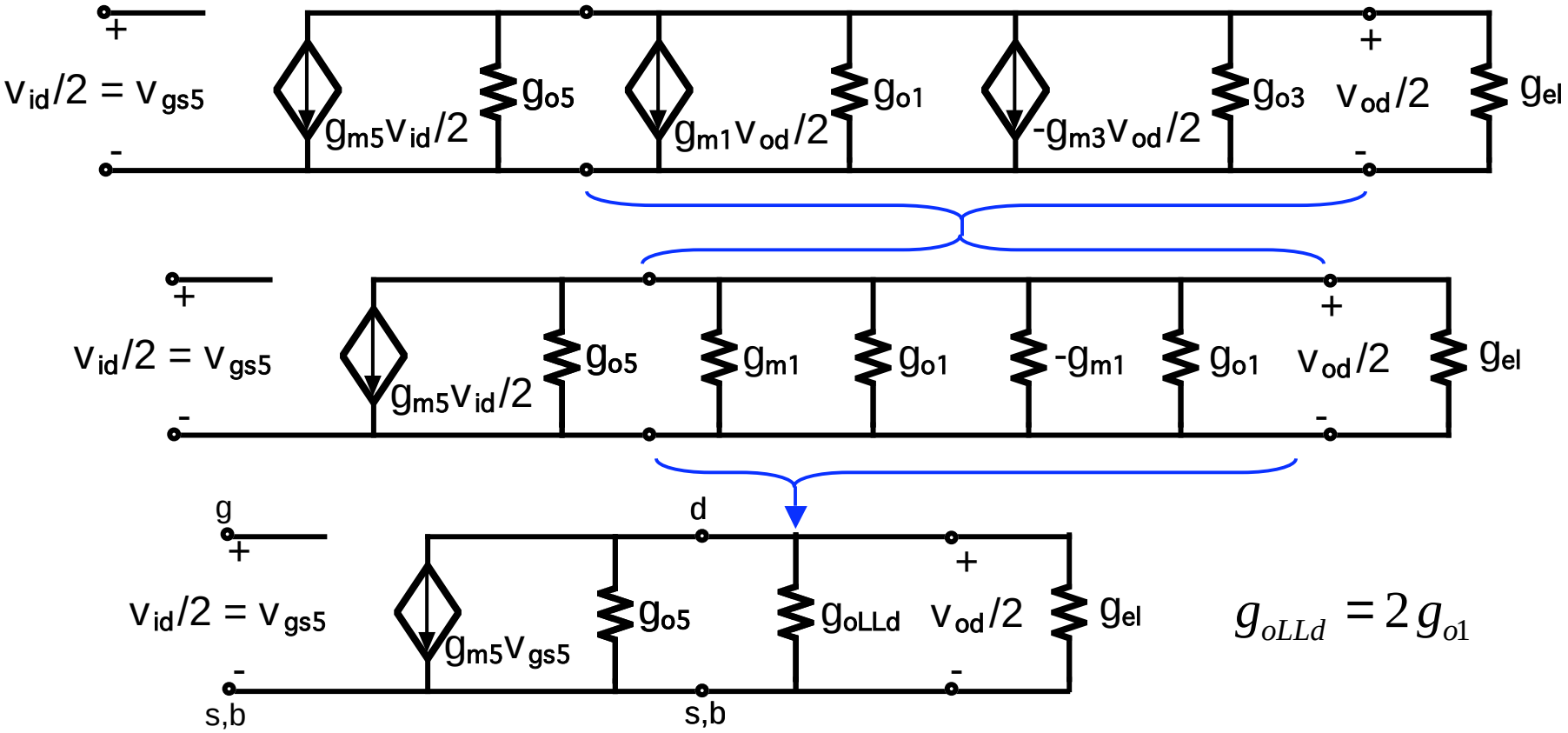


LEHC: difference-mode



The Lee load: analysis for difference-mode inputs, cont

LEHC: difference-mode



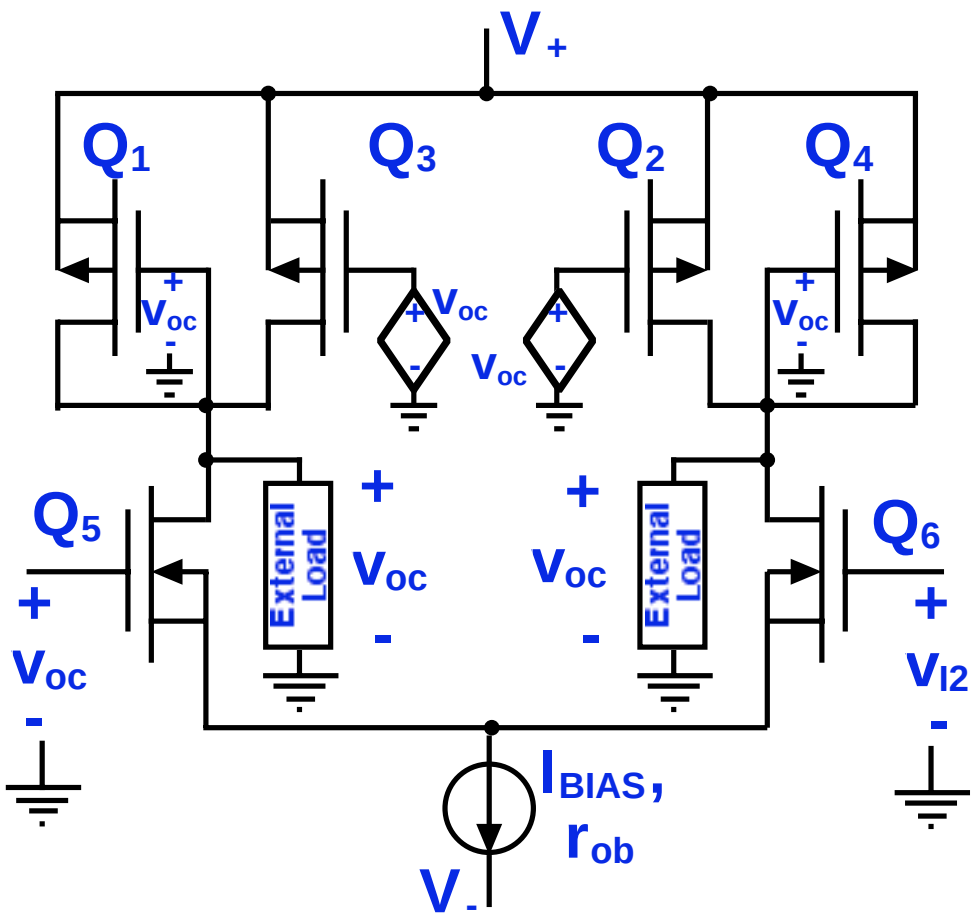
$$g_{oLLd} = 2\,g_{o1}$$

$$A_{vd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m5}}{\left(g_{o5} + 2g_{o1} + g_{e1}\right)}$$

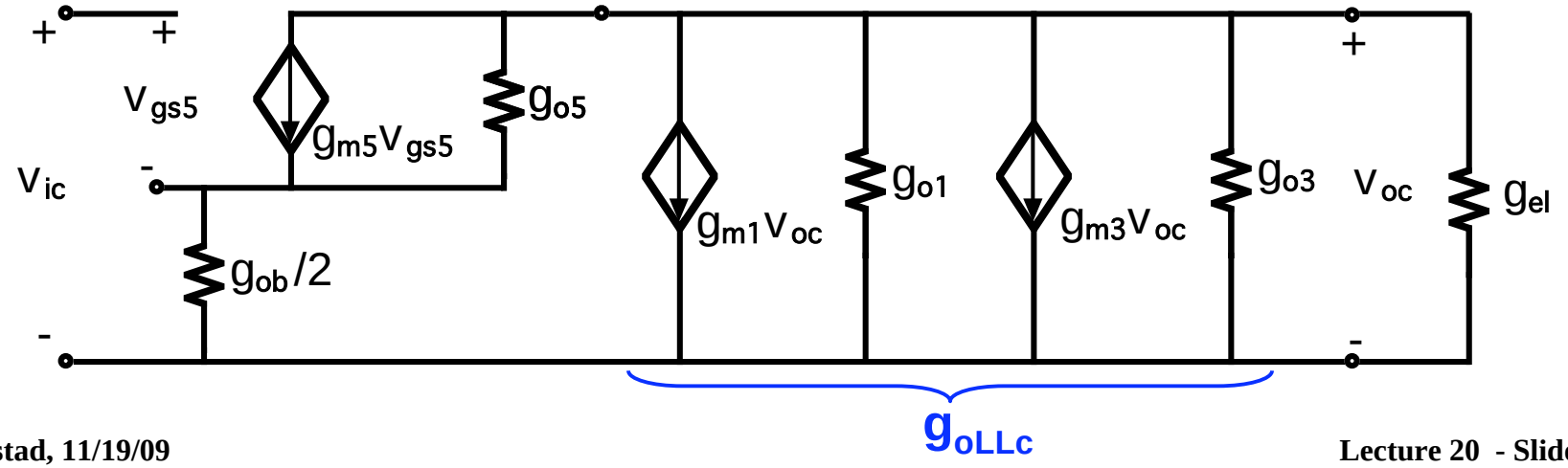
Note: In D.P., the outputs go to MOSFET gates so $g_{el} = 0$.

The Lee load:

analysis for common-mode inputs

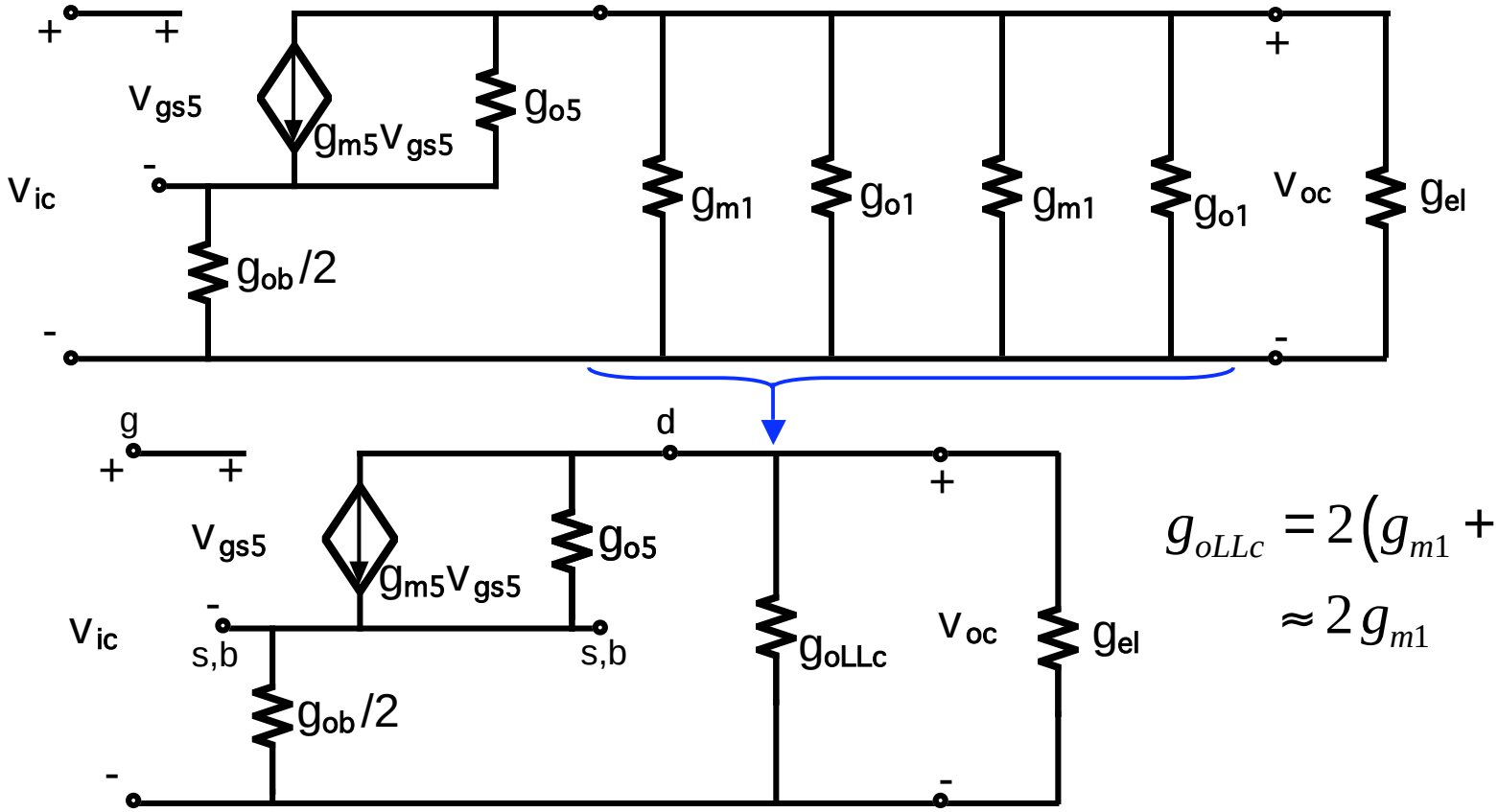


LEHC: common-mode



The Lee load: analysis for common-mode inputs, cont

LEHC: common-mode



$$g_{oLLc} = 2\left(g_{m1} + g_{o1}\right) \approx 2\,g_{m1}$$

$$A_{vc} = \frac{v_{oc}}{v_{ic}} = \frac{-g_{ob}}{2\left[2\left(g_{m1} + g_{o1}\right) + g_{e1}\right]} \approx -\frac{g_{ob}}{4g_{m1}}$$

Note: In D.P., the outputs go to MOSFET gates so $g_{el} = 0$.

Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

Maximum Gains	MOSFET (SI)	Bipolar-like (BJT and Sub-V_T MOS)
Linear resistor loads	$\leq \dfrac{2\left[I_D R_{SL}\right]_{\max}}{\left[v_{GS}-V_T\right]_{\min}}$	$\leq \dfrac{\left[I_C R_{SL}\right]_{\max}}{n V_t}$
Current source loads	$\leq \dfrac{2V_{A,eff}}{\left[v_{GS}-V_T\right]_{\min}}$	$\leq \dfrac{V_{A,eff}}{n V_t}$
Active loads		
Difference mode	$\propto \dfrac{2V_{A,eff}}{\left[v_{GS}-V_T\right]_{\min}}$	$\propto \dfrac{V_{A,eff}}{n V_t}$
Common mode	$\propto \dfrac{\left[v_{GS}-V_T\right]_{\min}}{2V_{A,bias}}$	$\propto \dfrac{n V_t}{V_{A,bias}}$

Observations:

- Non-linear (current source) loads typically yield much higher gain than linear resistors, i.e. $V_{A,eff} >> [I_D R_{SL}]_{max}$.
- The bias point is not as important to BJT-type stage gain.
- An SI MOSFET should be biased just above threshold for highest gain.
- For active loads what increases A_{vd}, decreases A_{vc}.

Achieving the maximum gain: $(v_{GS}-V_T)_{min}$ = ?

For SI-MOSFETs, maximizing the voltage gain (A_v or A_{vd}) requires minimizing ($V_{GS}-V_T$). What is the limit?

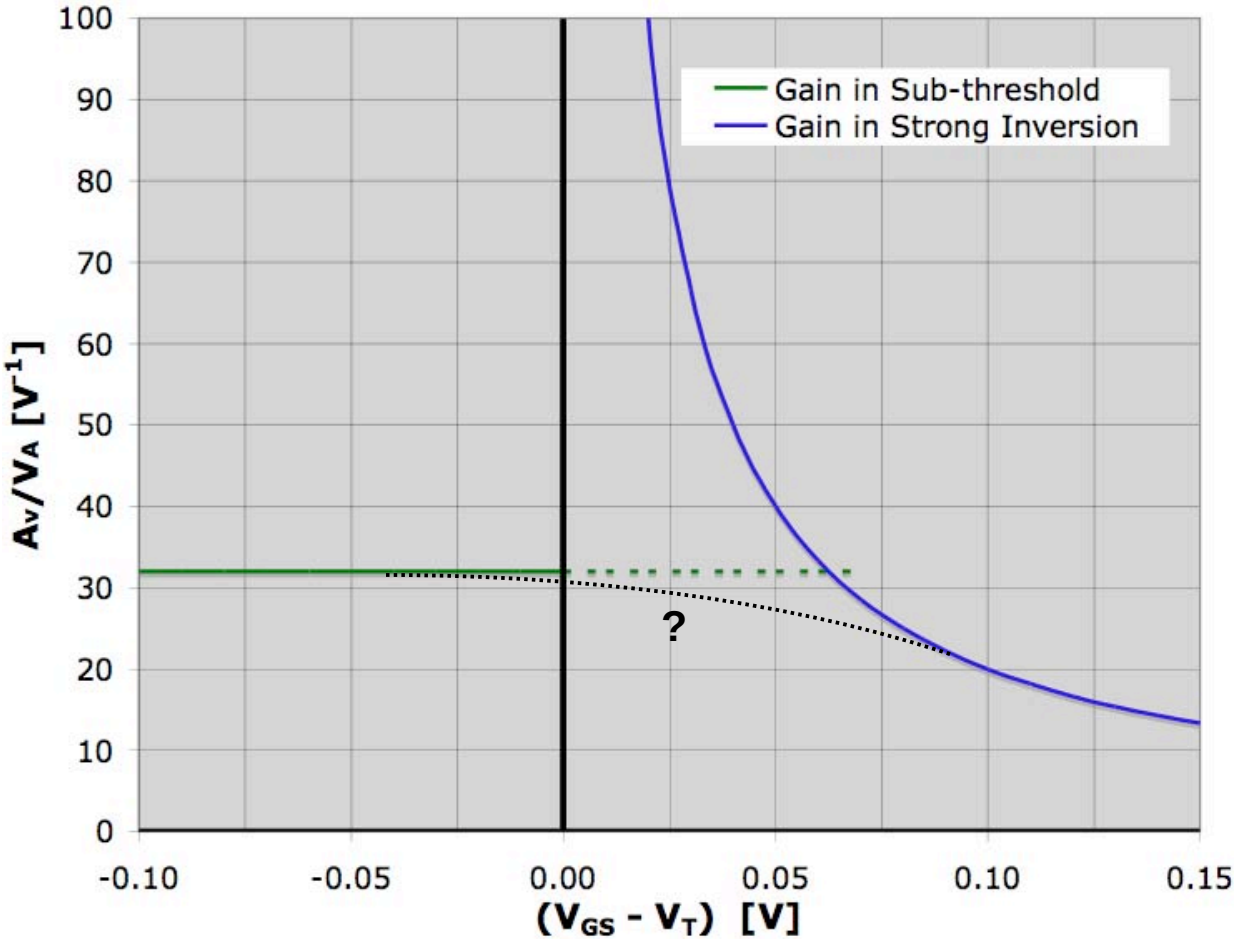
Sub-threshold:

$$\frac{A_v}{V_A} = \frac{1}{n\,V_t}$$

Strong inversion:

$$\frac{A_v}{V_A} = \frac{2}{(V_{GS} - V_T)}$$

A_v/V_A is a smooth curve, so clearly $(V_{GS}-V_T)_{min} > 2nV_t$.



Note: n = 1.25 was assumed.

Lecture 20 - Diff-Amp Analysis I - Summary

- **Performance metrics - specific to diff. amps.**
  - **Difference- and common-mode gains:** $A_{vd} = v_{od}/v_{id}$, $A_{vc} = v_{oc}/v_{ic}$
  - **Common-mode rejection ratio:** $CMRR = A_{vd}/A_{vc}$
  - **Common-mode input range**
- **Non-linear loads**
  - **Transistors biased in their constant current regions:**
    - MOSFETs in saturation
    - BJTs in their FAR
- **Active loads**
  - **Current mirror load:**
    - Achieves double- to single-ended conversion without loss of gain
    - Has high resistance for difference-mode signals
    - Has low resistance for common-mode signals
  - **Lee Load:**
    - Maintains differential signals
    - Has high resistance for difference-mode signals
    - Has low resistance for common-mode signals

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