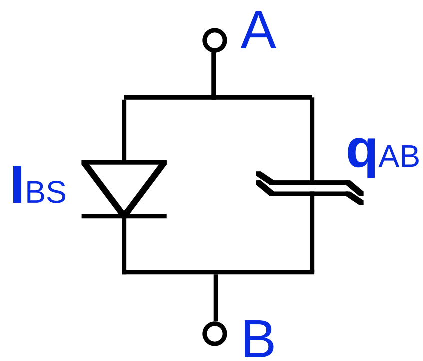
6.012 - Microelectronic Devices and Circuits

Lecture 17 - Linear Amplifier Basics; Biasing - Outline

- **Announcements**
  Announcements - Stellar postings on linear amplifiers
  Design Problem - Will be coming out next week, mid-week.
- **Review - Linear equivalent circuits**
  LECs: the same for npn and pnp; the same for n-MOS and p-MOS; all parameters depend on bias; maintaining a stable bias is critical
- **Biasing transistors**
  Current source biasing
  Transistors as current sources
  Current mirror current sources and sinks
- **The mid-band concept**
  Dealing with charge stores and coupling capacitors
- **Linear amplifiers**
  Performance metrics: gains (voltage, current, power)
  input and output resistances
  power dissipation
  bandwidth
  Multi-stage amplifiers and two-port analysis

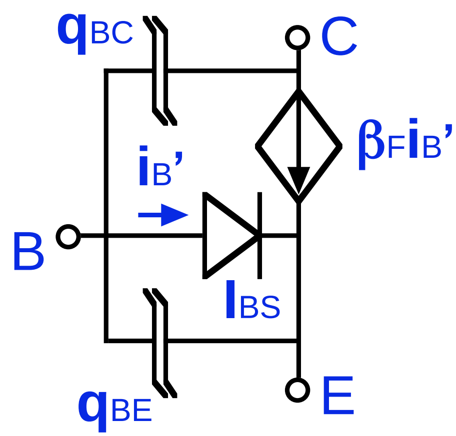
The large signal models:

p-n diode:



q_{AB}: Excess carriers on p-side plus excess carriers on n-side plus junction depletion charge.

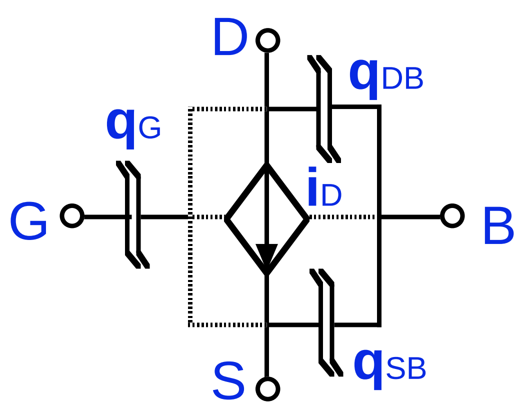
BJT: npn
(in F.A.R.)



q_{BE}: Excess carriers in base plus E-B junction depletion charge

q_{BC}: C-B junction depletion charge

MOSFET:
n-channel



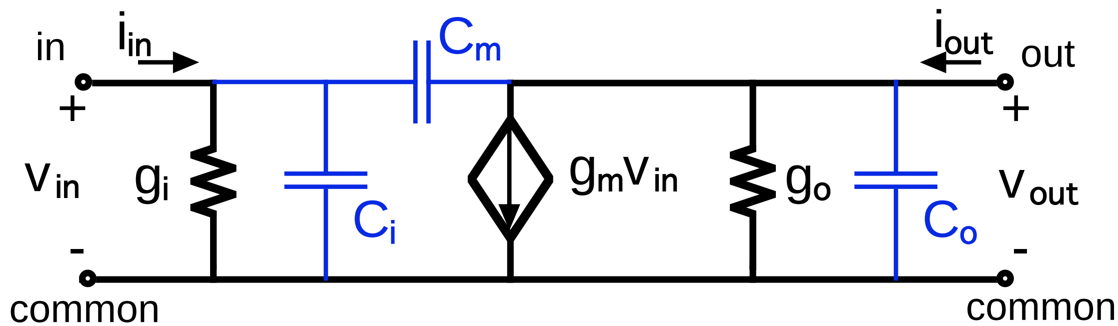
q_G: Gate charge; a function of v_{GS}, v_{DS}, and v_{BS}.

q_{DB}: D-B junction depletion charge

q_{SB}: S-B junction depletion charge

Reviewing our LECs: Important points made in Lec. 13

We found LECs for BJTs and MOSFETs in both strong inversion and sub-threshold. When $v_{bs} = 0$, they all look very similar:



Most linear circuits are designed to operate at frequencies where the capacitors look like open circuits. We can thus do our designs neglecting them.*

Bias dependences:

	BJT	ST MOS	SI MOS
g_i :	$qI_C/\beta_F kT$	0	0
g_m :	qI_C/kT	$qI_D/n\,kT$	$\sqrt{2KI_D/\alpha}$
g_o :	λI_C	λI_D	λI_D

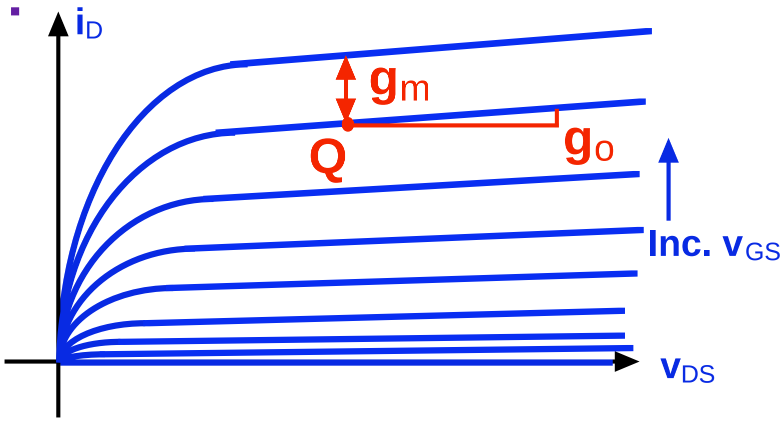
ST = sub-threshold
SI = strong inversion

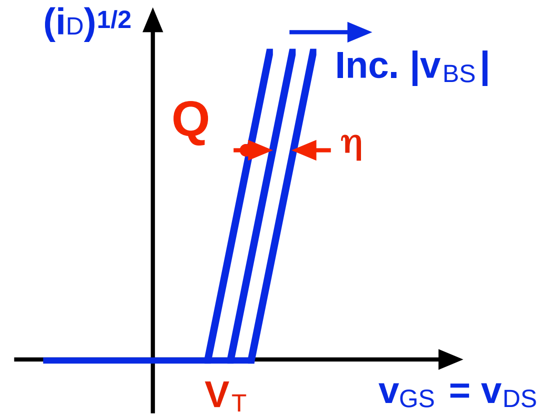
The LEC elements all depend on the bias levels. Establishing a known, stable bias point is a key part of linear circuit design. We use our large signal models in this design and analysis.

* Only when we want to determine the maximum frequency to which our designs can usefully operate must we include the capacitors.

LECs: Identifying the incremental parameters in the characteristics

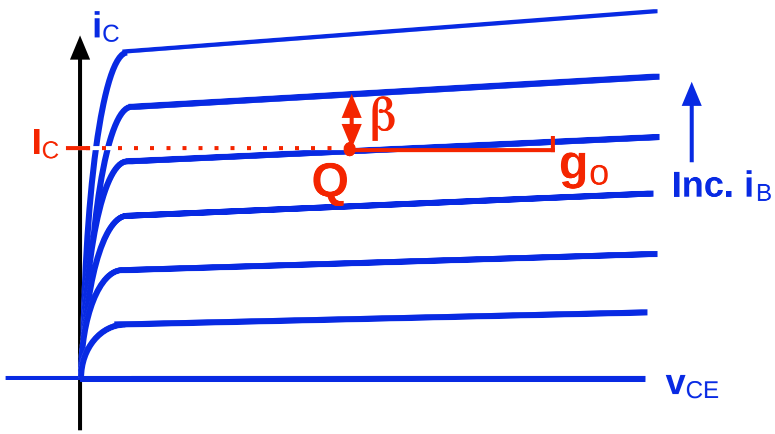
MOSFET:

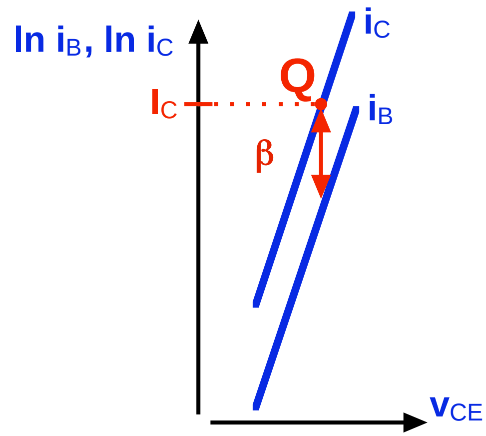




$$g_m = di_D/dv_{GS}|_Q;\ g_{mb} = \eta g_m \text{ with } \eta = -dV_T/dv_{BS}|_Q;\ g_o = di_D/dv_{DS}|_Q$$

BJT:



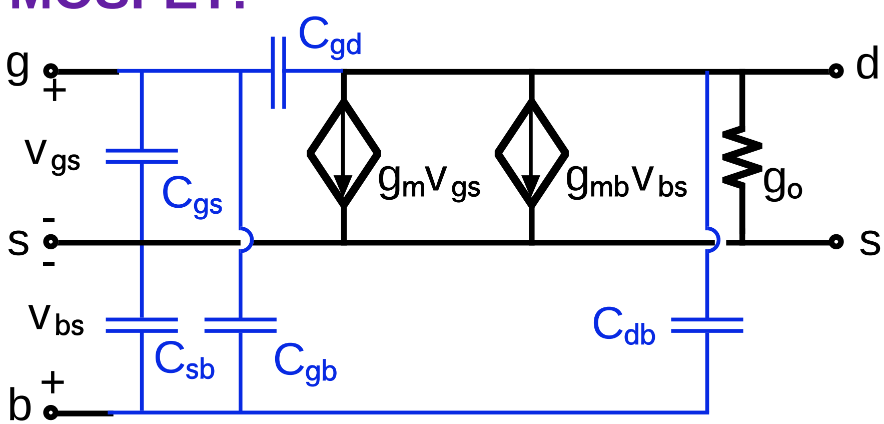


$$g_m = qI_C/kT;\ g_\pi = \beta g_m \text{ with } \beta = di_C/di_B|_Q;\ g_o = di_C/dv_{CE}|_Q$$

Linear equivalent circuits for transistors (dynamic):

Collecting our results for the MOSFET and BJT biased in FAR

MOSFET:



$$g_m = K\left[V_{GS} - V_T(V_{BS})\right]\left[1 + \lambda V_{DS}\right] \approx \sqrt{2K\,I_D}$$

$$g_o = \frac{K}{2}\left[V_{GS} - V_T(V_{BS})\right]^2 \lambda \approx \lambda I_D = \frac{I_D}{V_A}$$

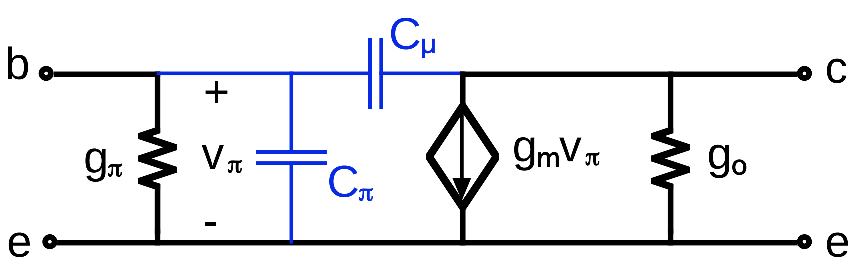
$$g_{mb} = \eta\, g_m = \eta \sqrt{2K\,I_D}$$

$$\text{with} \quad \eta \equiv -\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{Si} q N_A}{\left|q\phi_p\right| - V_{BS}}}$$

$C_{gs} = \frac{2}{3} W\,L\,C_{ox}^*,$ $\quad C_{sb}, C_{gb}, C_{db}$: depletion capacitances

$C_{gd} = W\,C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

BJT:



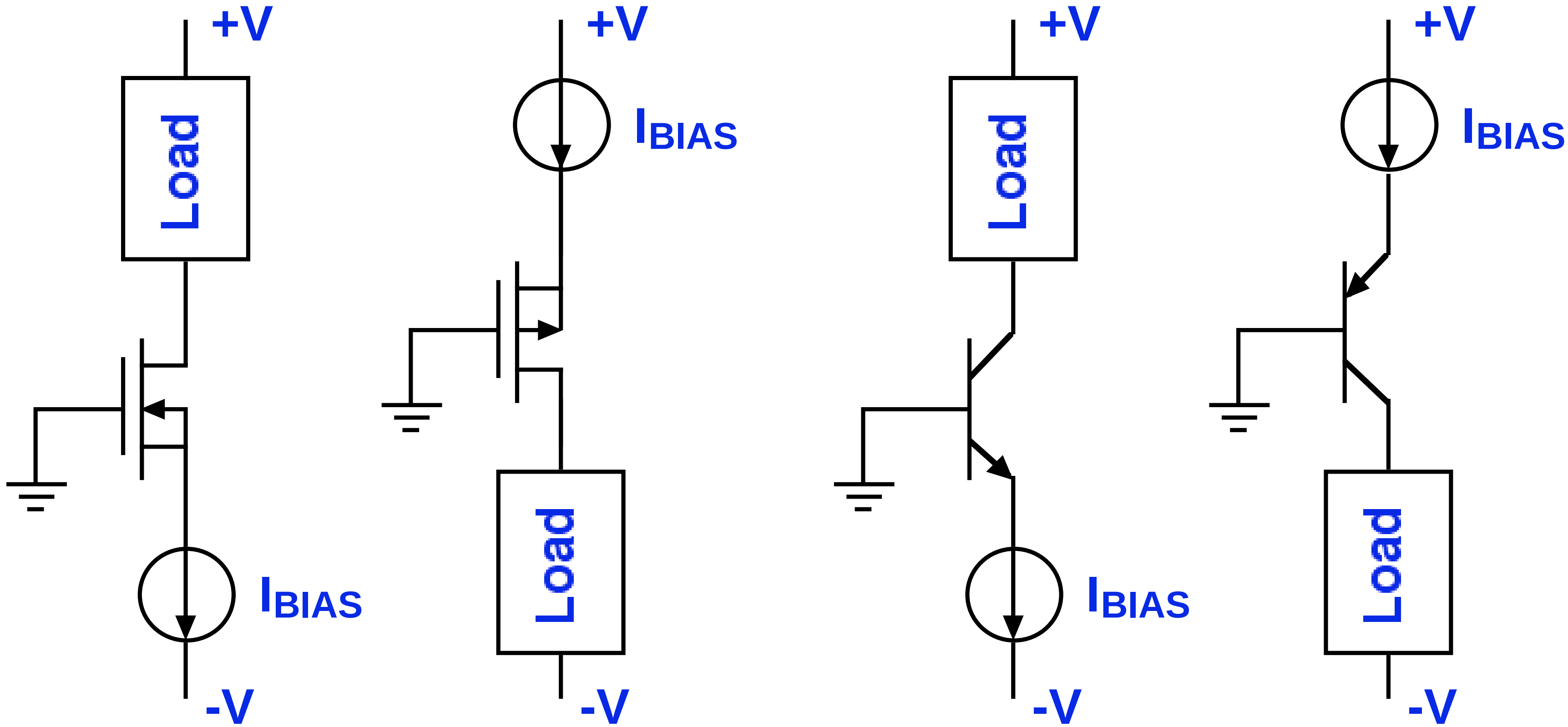
$$g_m = \frac{q}{kT}\beta_o I_{BS}\, e^{qV_{BE}/kT}\left[1 + \lambda V_{CE}\right] \approx \frac{qI_C}{kT}$$

$$g_\pi = \frac{g_m}{\beta_o} = \frac{qI_C}{\beta_o\, kT}$$

$$g_o = \beta_o I_{BS}\left[e^{qV_{BE}/kT} + 1\right]\lambda \approx \lambda I_C = \frac{I_C}{V_A}$$

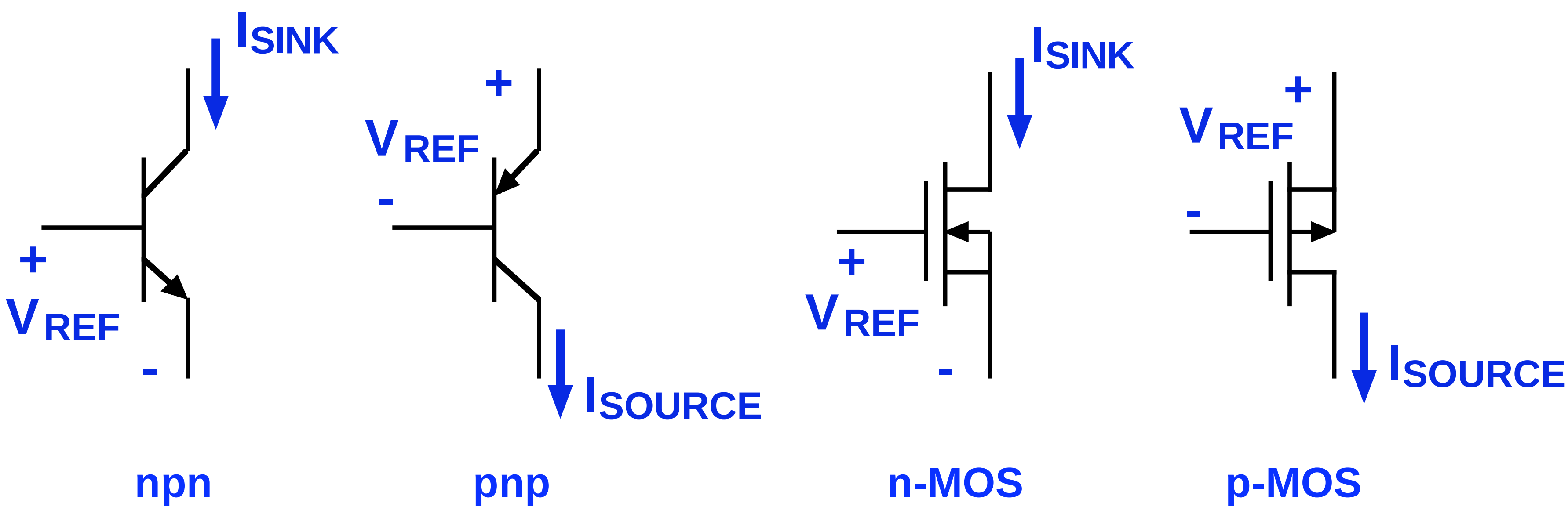
$C_\pi = g_m \tau_b +$ B-E depletion cap. with $\tau_b \equiv \frac{w_B^2}{2D_e}$, $\quad C_\mu$: B-C depletion cap.

MOSFETs and BJTs biased for use in linear amplifiers



n-MOS p-MOS npn pnp

Getting I_{BIAS}: Making a transistor into a current source/sink*



BJT current sources/sinks

Must maintain V_{CE} > 0.2V
[V_{EC} in case of pnp]

$$I_{SOURCE/SINK} = [\beta_F/(\beta_F+1)]\, I_{ES}(e^{qV_{REF}/kT}-1)$$
$$\approx I_{ES}e^{qV_{REF}/kT}$$

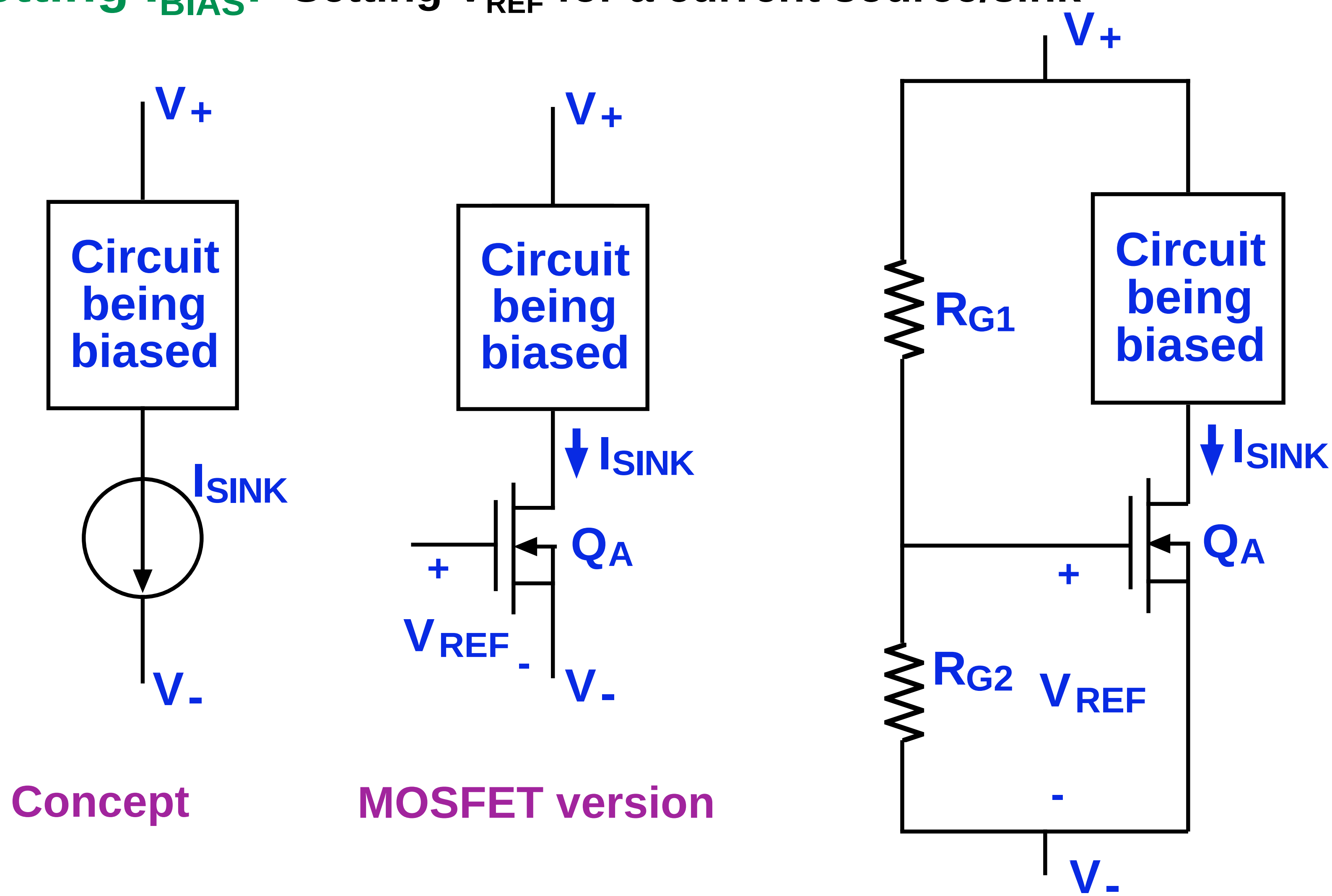
MOSFET current sources/sinks

Must maintain $V_{DS} > (V_{REF} - V_T)$
[$V_{SD} > (V_{REF} + V_T)$ in case of p-MOS]

$$I_{SOURCE/SINK} = K(V_{REF} - |V_T|)^2/2$$

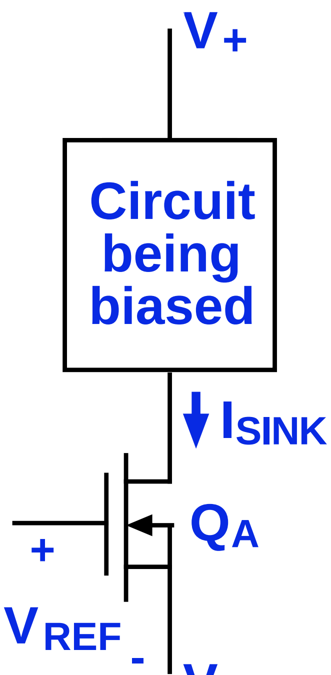
* Some people make a distinction between a "sink" and a "source"; you can call them all "sources" if you wish.

Getting I_{BIAS}: Setting V_{REF} for a current source/sink

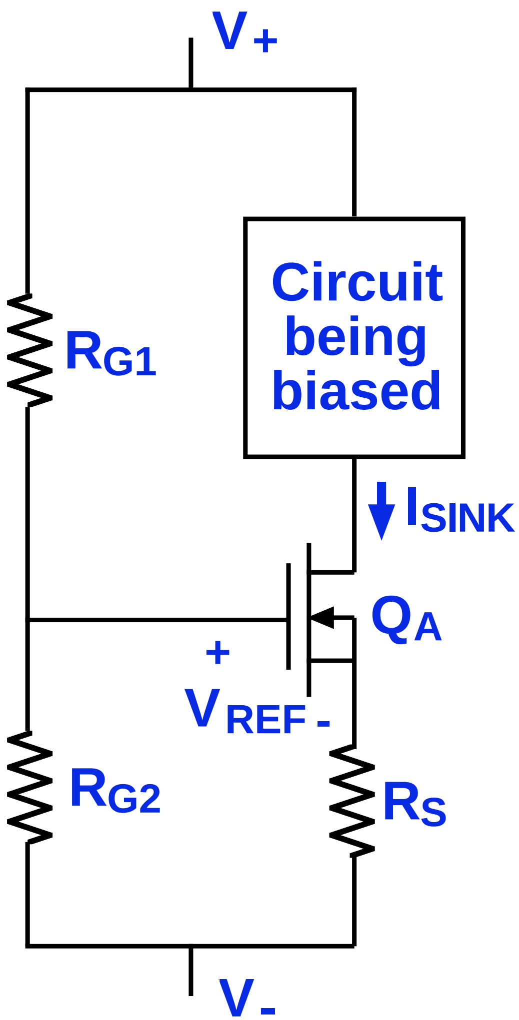


Simple resistor divider: too sensitive to device to device variations of V_T, K

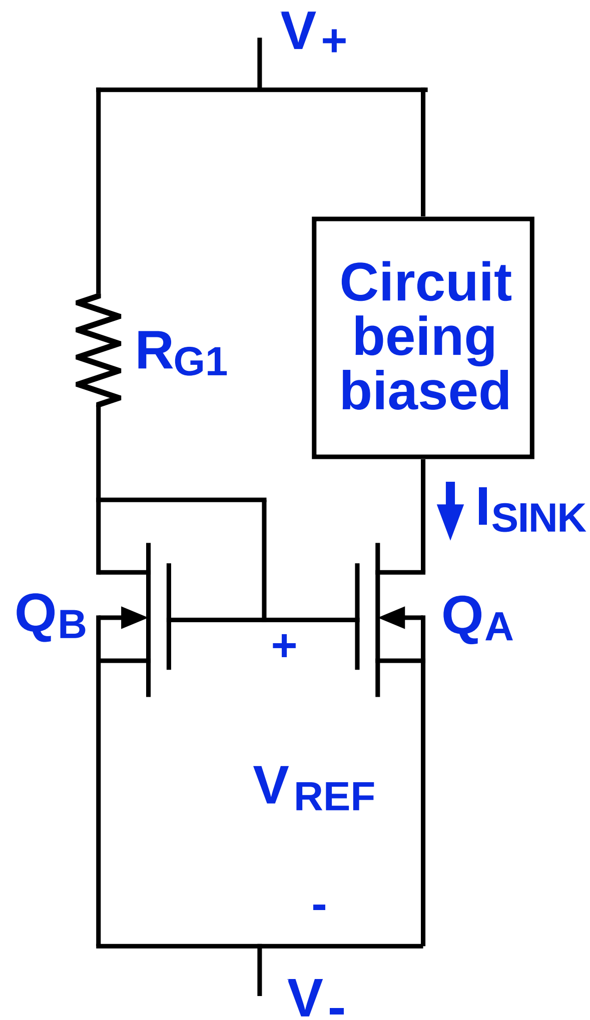
Getting I_{BIAS}: Setting V_{REF}, cont.



MOSFET version



Divider with R_G: less sensitive to variations in V_T, K, but not perfect; resistors are undesirable

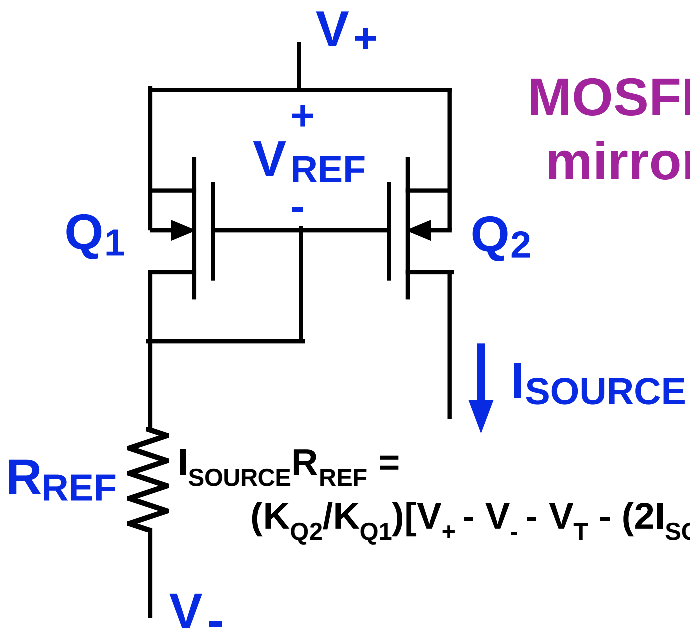


Current Mirror: matches V_T, K variations; easy to bias multiple stages; only 1 R*

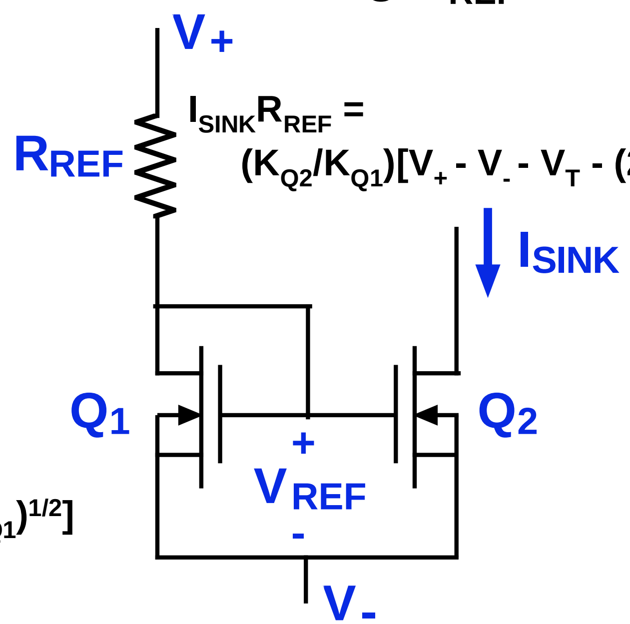
* We'll see how to make this zero..

Current mirror sources/sinks: establishing V_{REF}; setting I

MOSFET mirrors

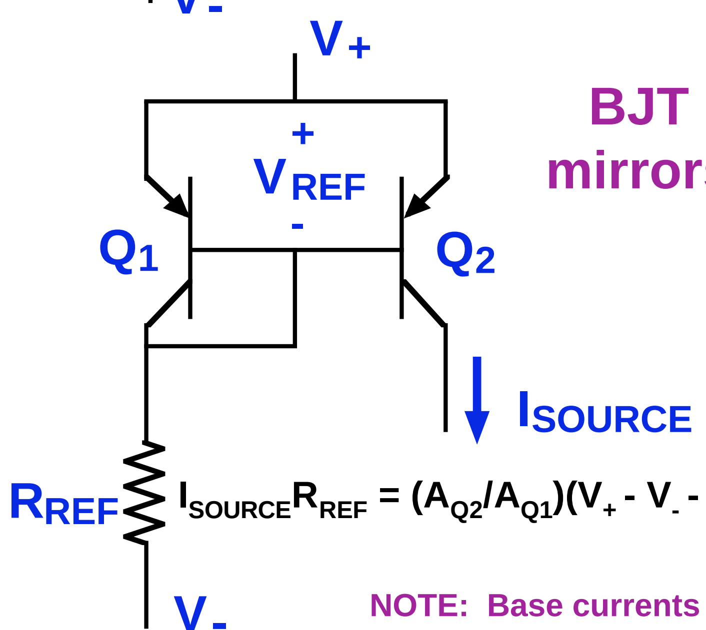


$I_{SOURCE}R_{REF} = (K_{Q2}/K_{Q1})[V_+ - V_- - V_T - (2I_{SOURCE}/K_{Q1})^{1/2}]$

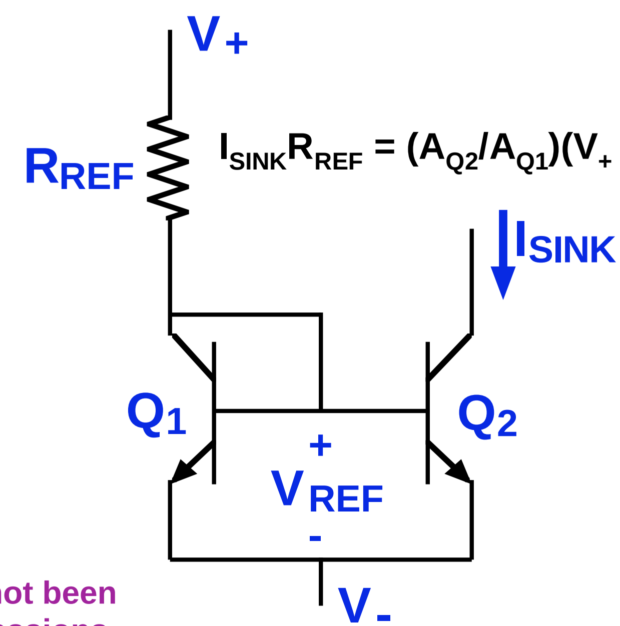


$I_{SINK}R_{REF} = (K_{Q2}/K_{Q1})[V_+ - V_- - V_T - (2I_{SINK}/K_{Q1})^{1/2}]$

BJT mirrors



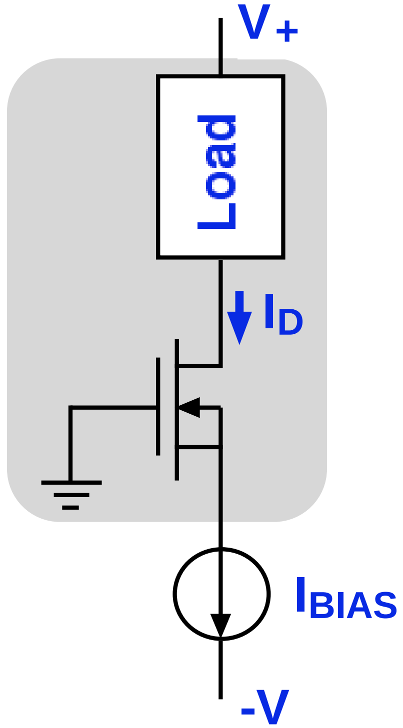
$I_{SOURCE}R_{REF} = (A_{Q2}/A_{Q1})(V_+ - V_- - 0.6)$



$I_{SINK}R_{REF} = (A_{Q2}/A_{Q1})(V_+ - V_- - 0.6)$

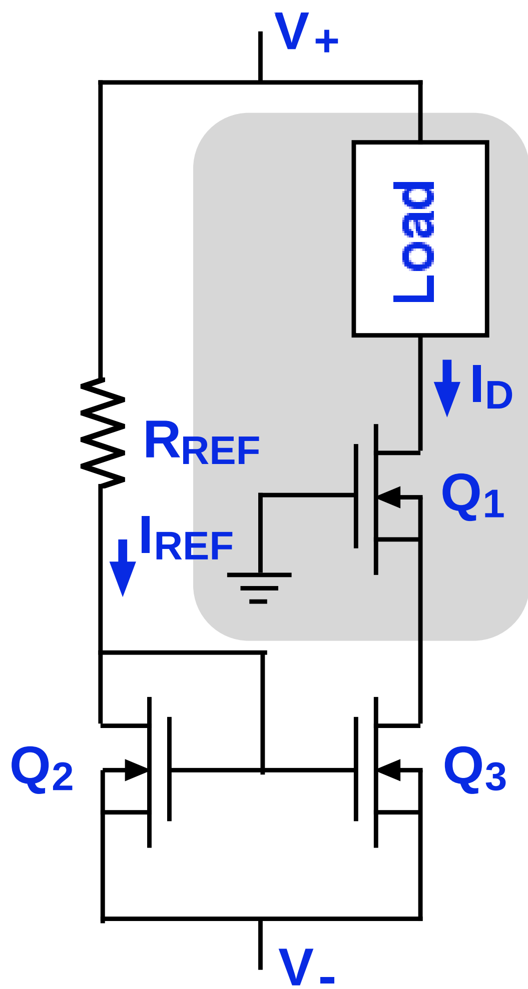
NOTE: Base currents have not been accounted for in these expressions

Examples of current mirror biased MOSFET circuits:



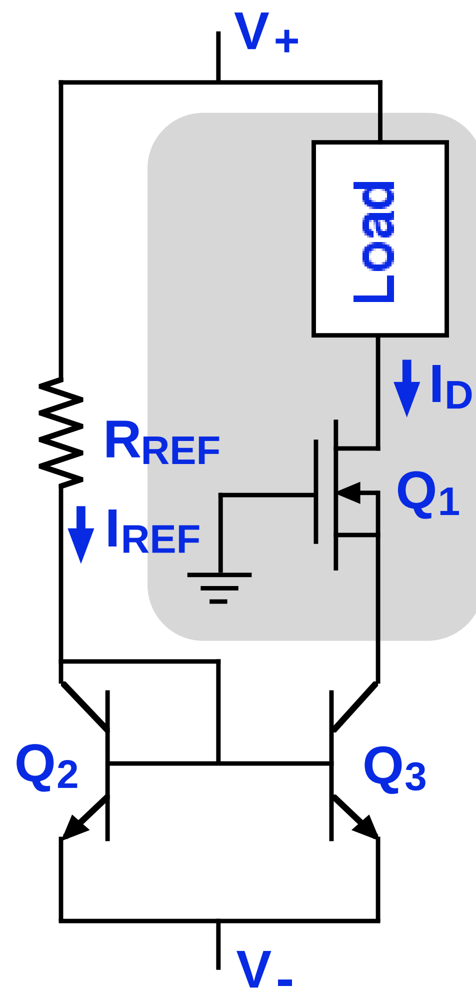
Above: Concept

Right: Implementations



MOSFET Mirror

$I_D \approx (K_{Q3}/K_{Q2})\ I_{REF}$



BJT Mirror

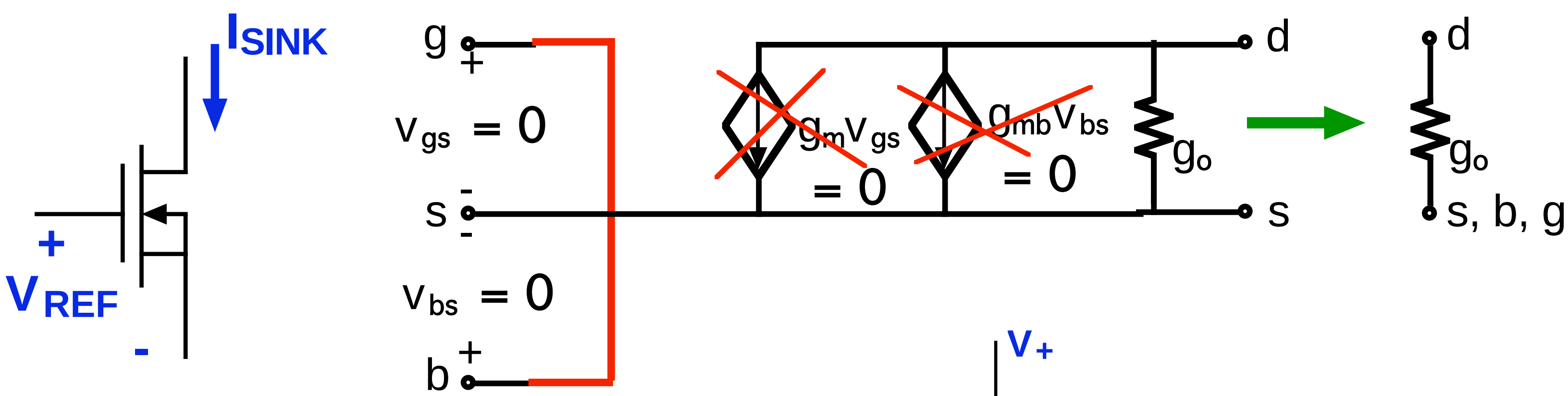
$I_D \approx (A_{Q3}/A_{Q2})\ I_{REF}$

Final comment on current sources:

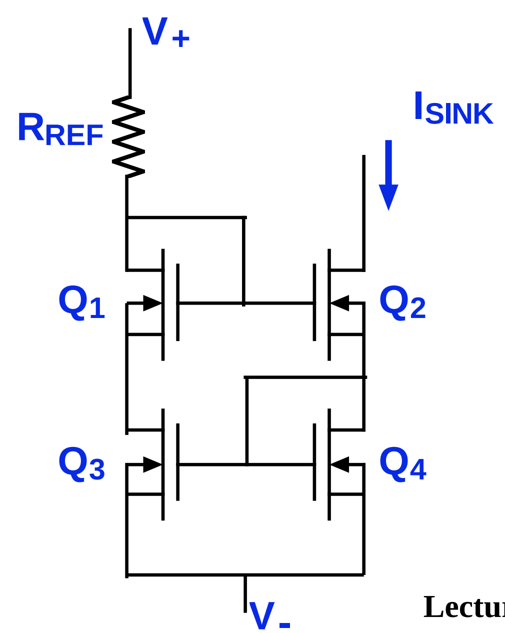
What do they look like incrementally?

They look like a resistor with conductance g_o

For example, consider an n-MOS sink:



How do you do better (smaller g_o)?
The <u>cascode</u> connection:

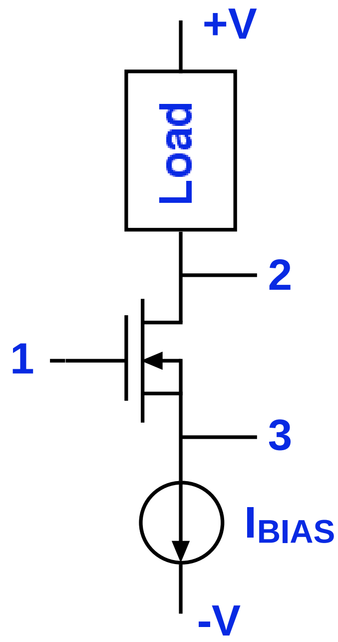


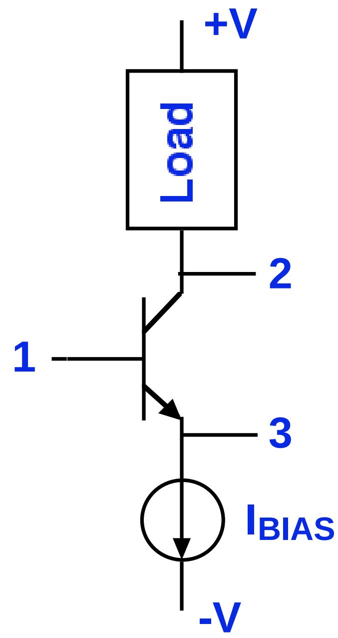
- check it out for yourself
- we'll come back to the cascode in Lec. 22

Linear amplifier layouts: The practical ways of putting inputs to, and taking outputs from, transistors to form linear amplifiers

There are 12 choices: three possible nodes to connect to the input, and for each one, two nodes from which to take an output, and two choices of what to do with the remaining node (ground it or connect it to something).

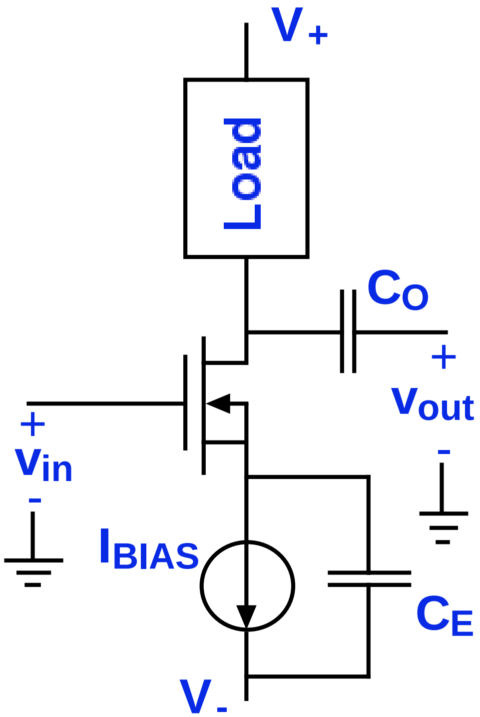
Not all these choices work well, however. In fact only three do:



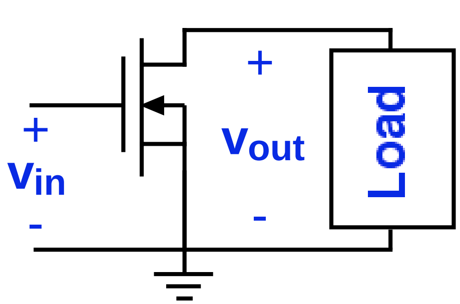


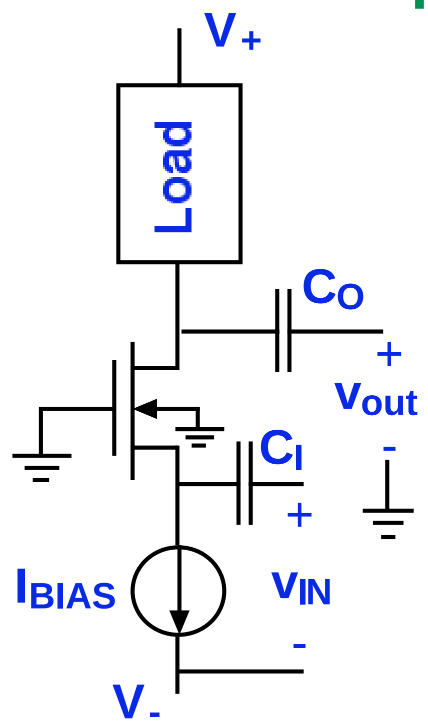
Name	Input	Output	Grounded
Common source/emitter	1	2	3
Common gate/base	3	2	1
Common drain/collector (Source/emitter follower)	1	3	2
Source/emitter degeneration	1	2	none

- **Three MOSFET single-transistor amplifiers**

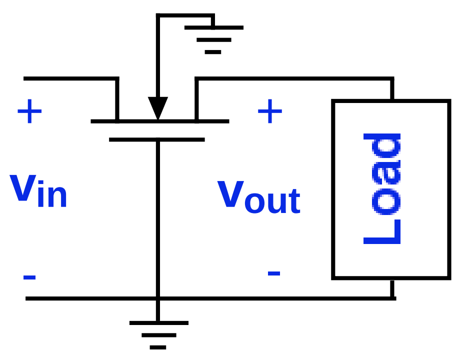


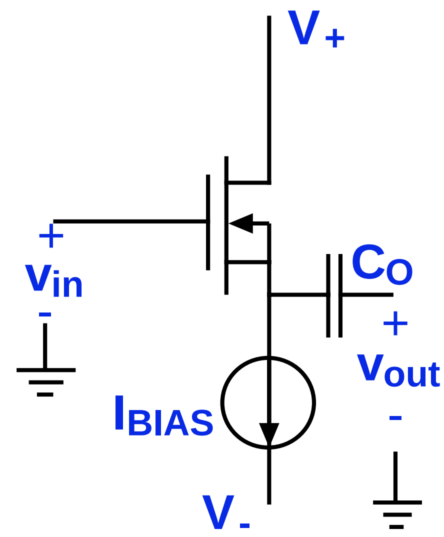
COMMON SOURCE
Input: gate
Output: drain
Common: source
Substrate: to source



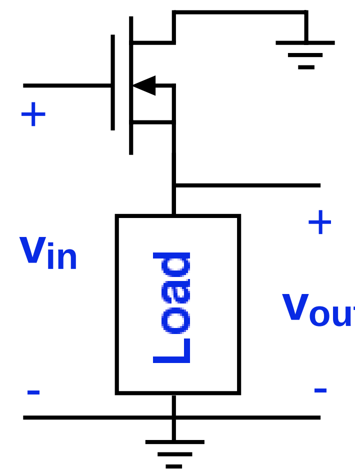


COMMON GATE
Input: source; Output: drain
Common: gate
Substrate: to ground

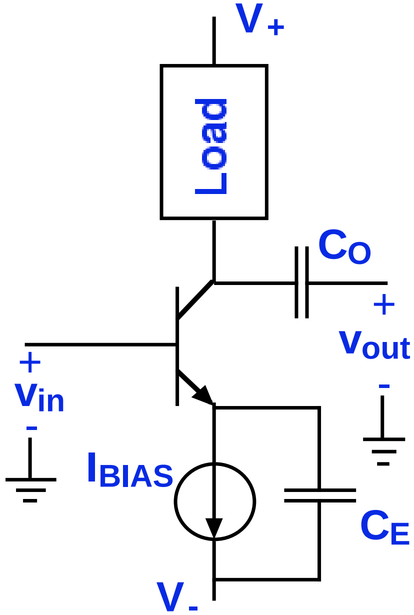




SOURCE FOLLOWER
Input: gate
Output: source
Common: drain
Substrate: to source

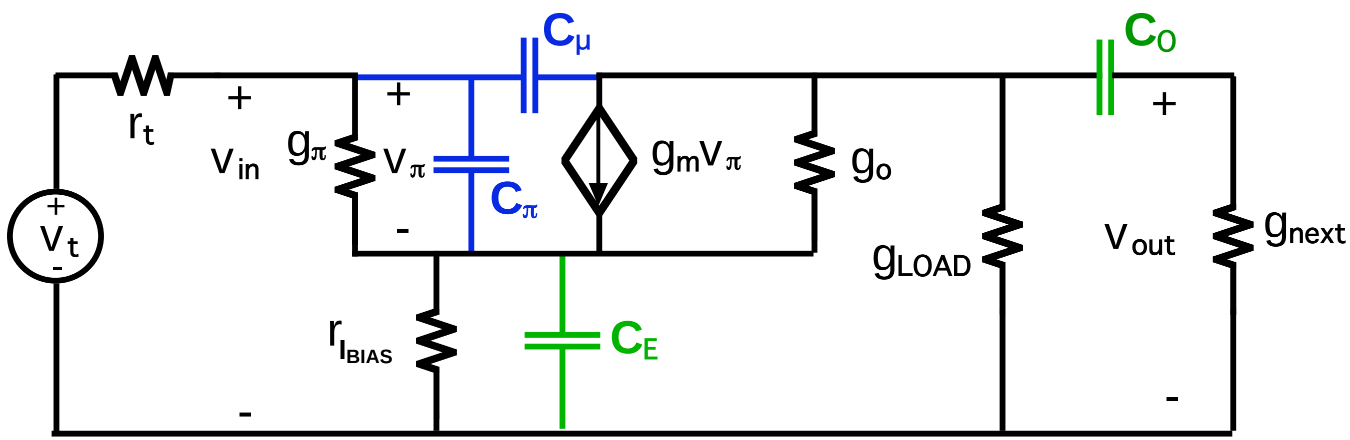


Mid-band: the frequency range of constant gain and phase



Common emitter example:

The linear equivalent circuit for the common emitter amplifier stage on the left is drawn below with all of the elements included:



The capacitors are of two types:

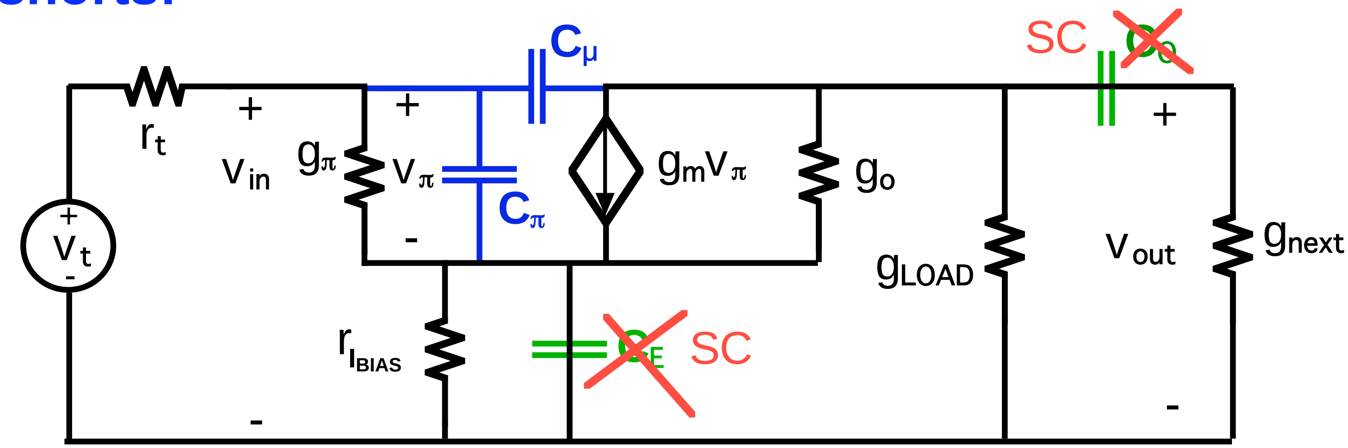
Biasing capacitors: they are typically very large (in μF range)
(C_O, C_E, etc.) they will be effective shorts above some ω_{LO}

Device capacitors: they are typically very small (in pF range)
(C_π, C_μ, etc.) they will be effective open circuits below some ω_{HI}

Mid-band, cont.

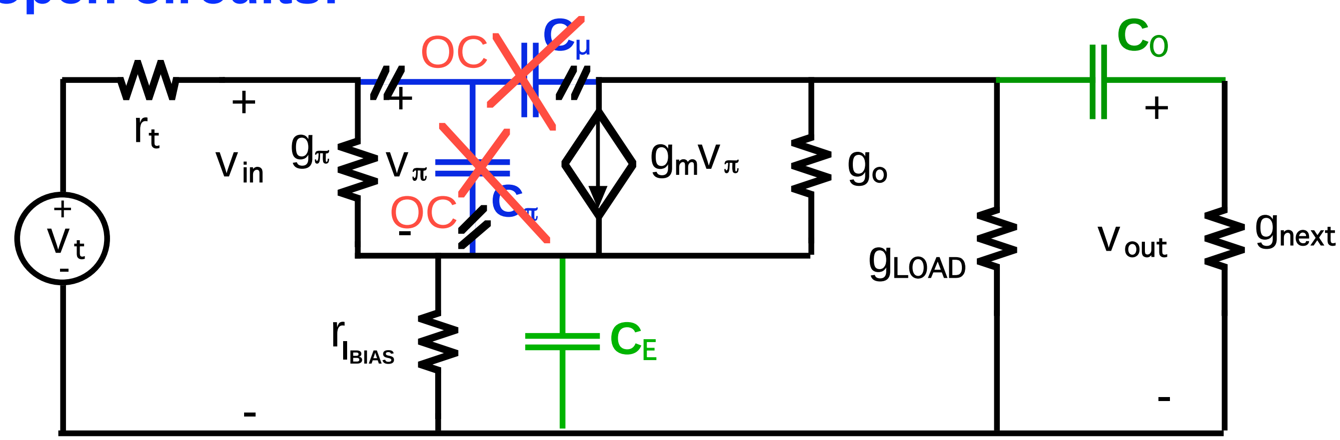
At frequencies <u>above</u> some value ($\equiv \omega_{LO}$) the biasing capacitors look like shorts:

$\omega_{LO} < \omega$



At frequencies <u>below</u> some value ($\equiv \omega_{HI}$) the device capacitors look like open circuits:

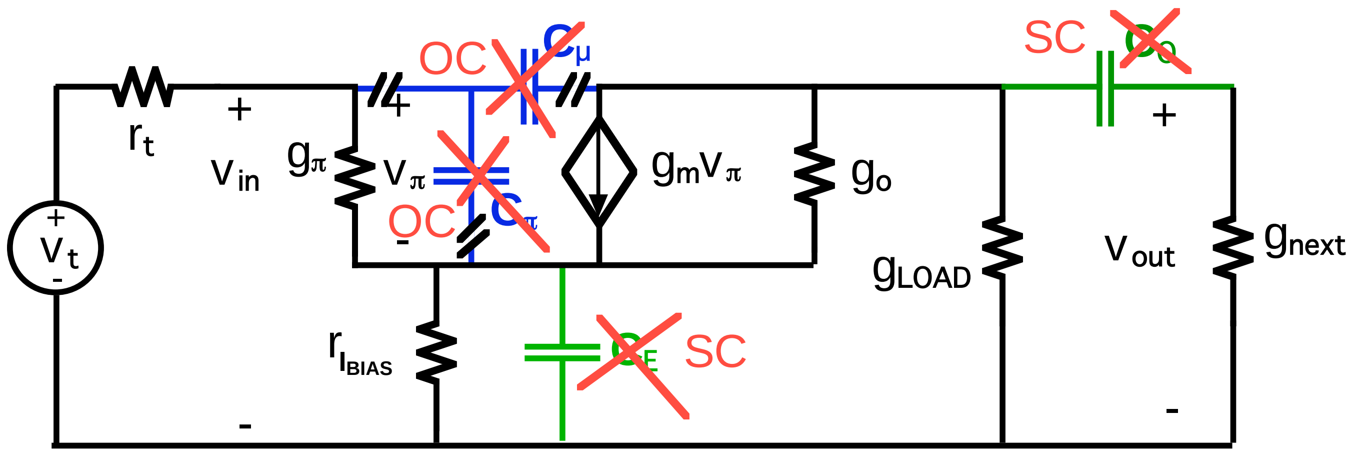
$\omega < \omega_{HI}$



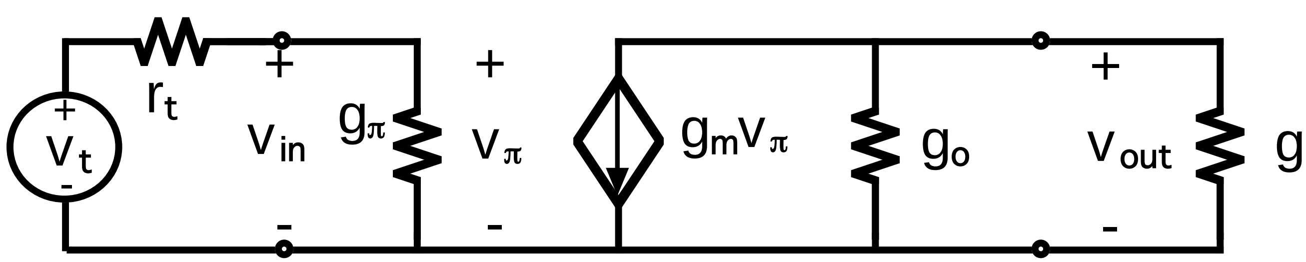
Mid-band, cont.

If $\omega_{LO} < \omega_{HI}$, then there is a range of frequencies where all of the capacitors are either short circuits (the biasing capacitors) or open circuits (the device capacitors), and we have:

$\omega_{LO} < \omega < \omega_{HI}$



We call the frequency range between ω_{LO} and ω_{HI}, the "mid-band" range. For frequencies in this range our model is simply:

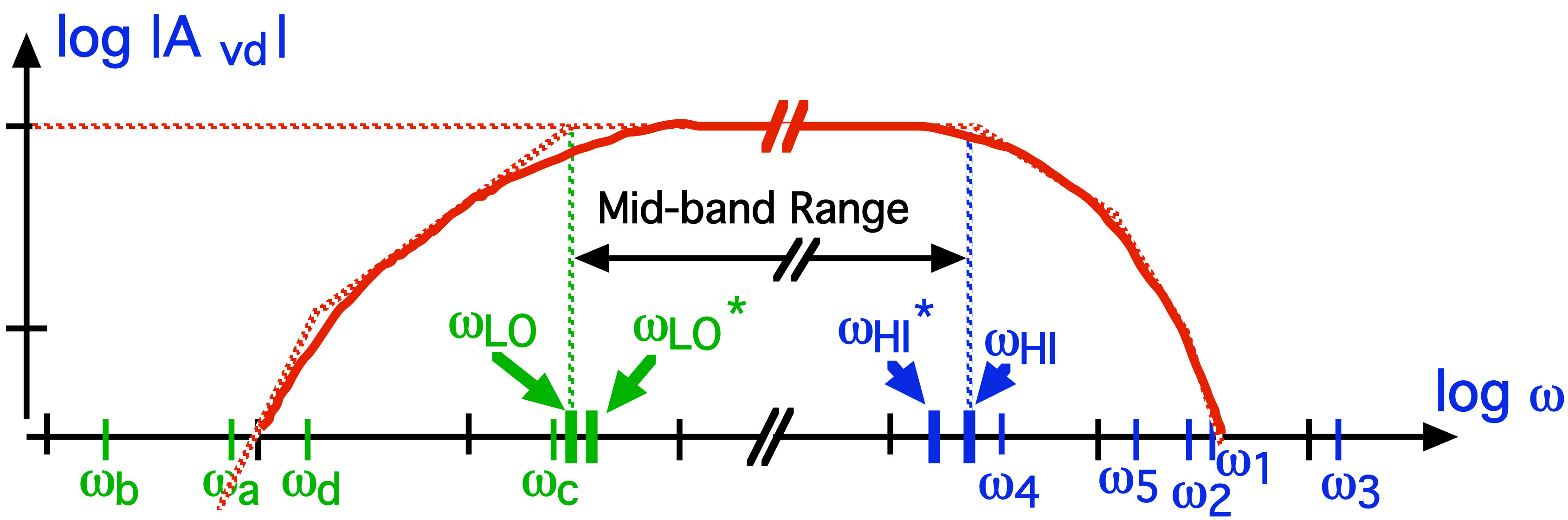


($\equiv g_{LOAD} + g_{next}$)

Valid for $\omega_{LO} < \omega < \omega_{HI}$, the "mid-band" range, where all bias capacitors are shorts and all device capacitors are open.

Mid-band, cont: The mid-band range of frequencies

In this range of frequencies the gain is a constant, and the phase shift between the input and output is also constant (either 0˚ or 180˚).



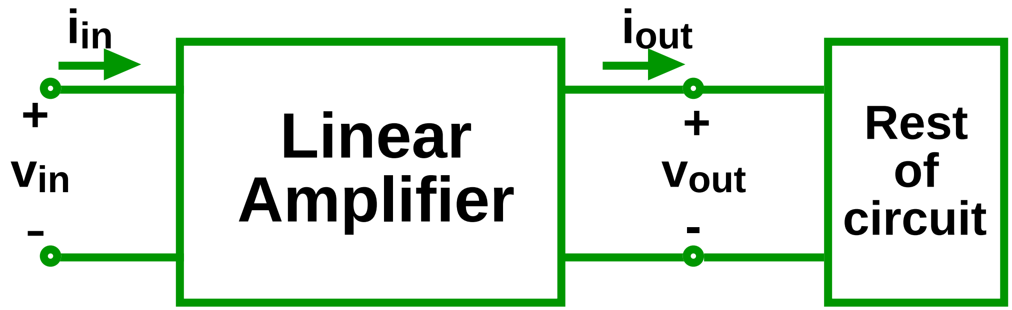
All of the <u>parasitic and intrinsic device capacitances</u> are effectively open circuits

All of the <u>biasing and coupling capacitors</u> are effectively short circuits

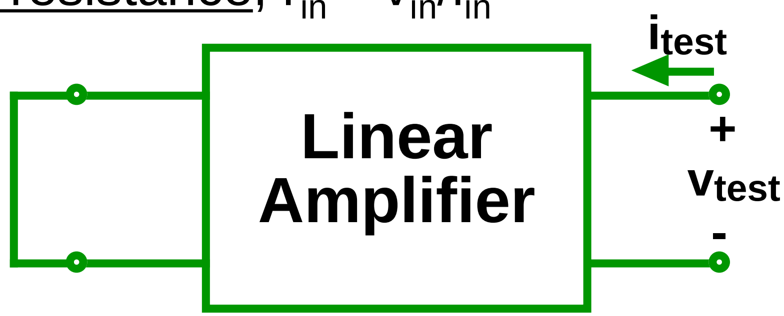
*** We will learn how to estimate ω_{HI} and ω_{LO} in Lectures 23/24.**

Linear amplifier basics: performance metrics

The characteristics of linear amplifiers that we use to compare different amplifier designs, and to judge their performance and suitability for a given application are given below:



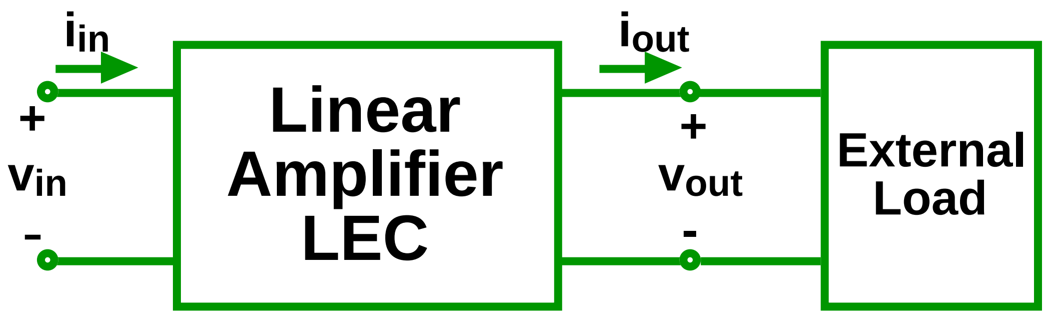
<u>Voltage gain</u>, $A_v = v_{out}/v_{in}$
<u>Current gain</u>, $A_i = i_{out}/i_{in}$
<u>Power gain</u>, $A_{power} = P_{out}/P_{in} = v_{out}i_{out}/v_{in}i_{in} = A_vA_i$
<u>Input resistance</u>, $r_{in} = v_{in}/i_{in}$



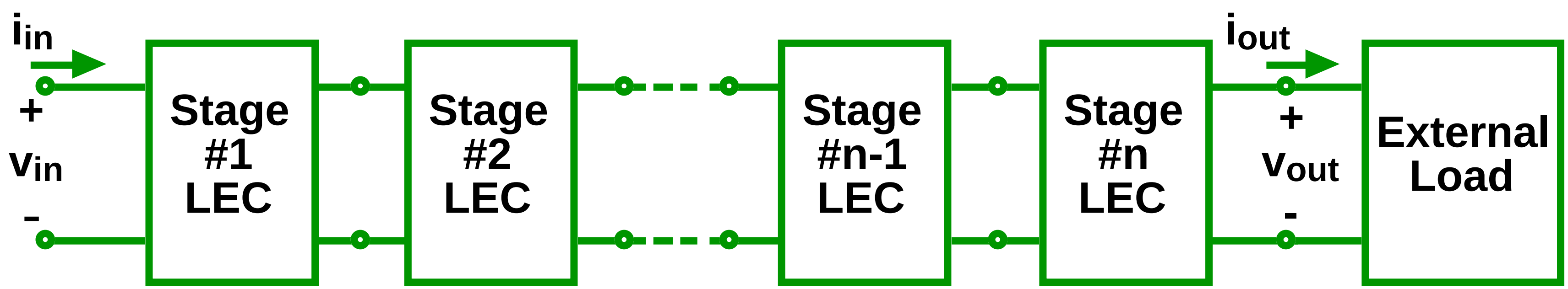
<u>Output resistance</u>, $r_{out} = v_{test}/i_{test}$ with $v_{in} = 0$

<u>DC Power dissipation</u>, $P_{DC} = (V_+ - V_-)(\Sigma I_{BIAS}\text{'s})$

Linear amplifier basics: multi-stage structure; two-ports



The typical linear amplifier is comprised of multiple building-block stages, often such as the single transistor stages we introduced on Slide 14 (and which will be the topic of Lect. 19):

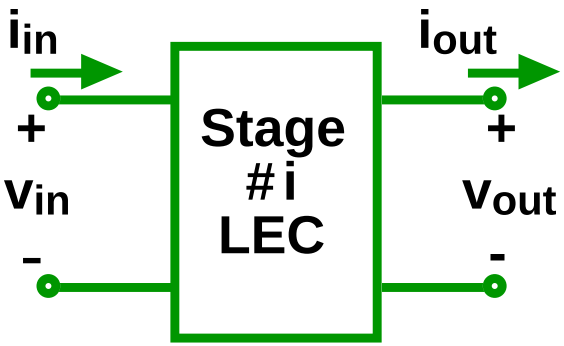


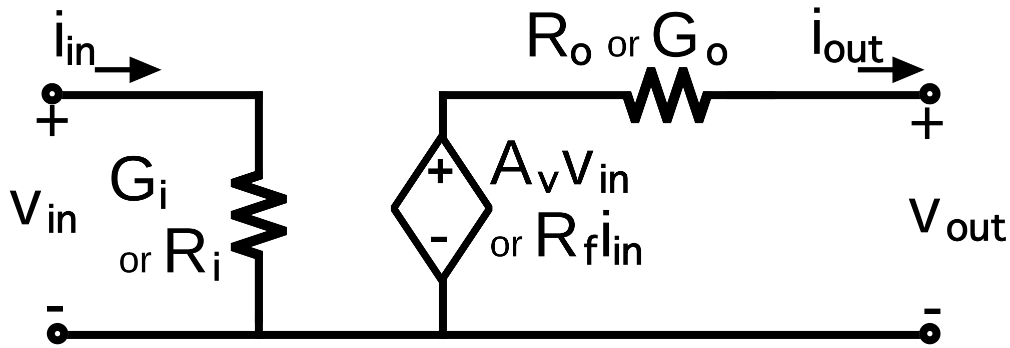
A useful concept and tool for analyzing, as well as designing, such multi-stage amplifiers is the two-port representation.

Note: More advanced multi-stage amplifiers might include feedback, the coupling of the outputs of some stages to the inputs of preceding stages. This is not shown in this figure.

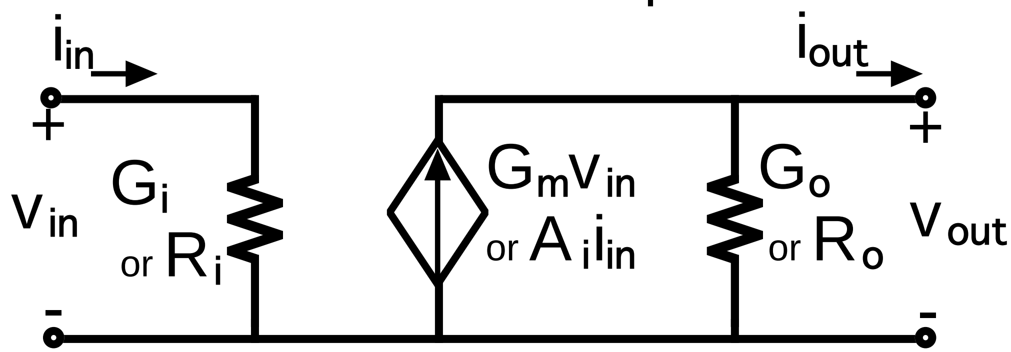
Linear amplifier basics: two-port representations

Each building block stage can be represented by a "two-port" model with either a Thévenin or a Norton equivalent at its output:



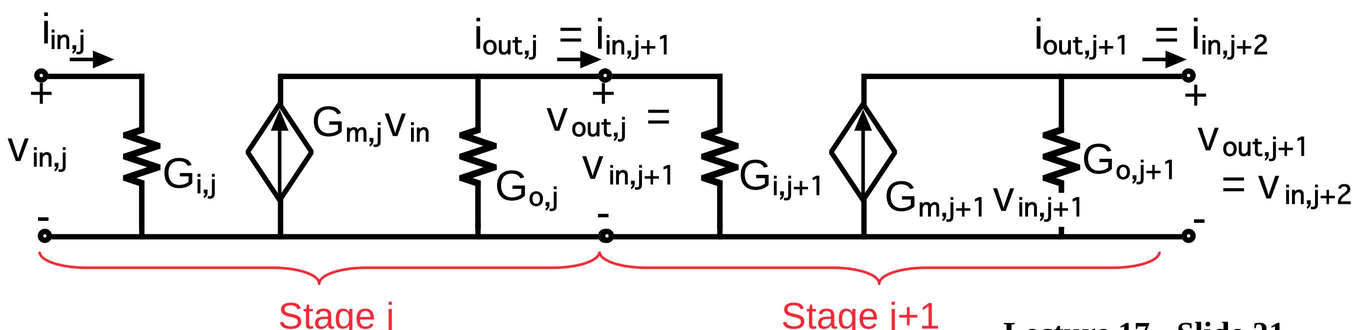


Thévenin Output

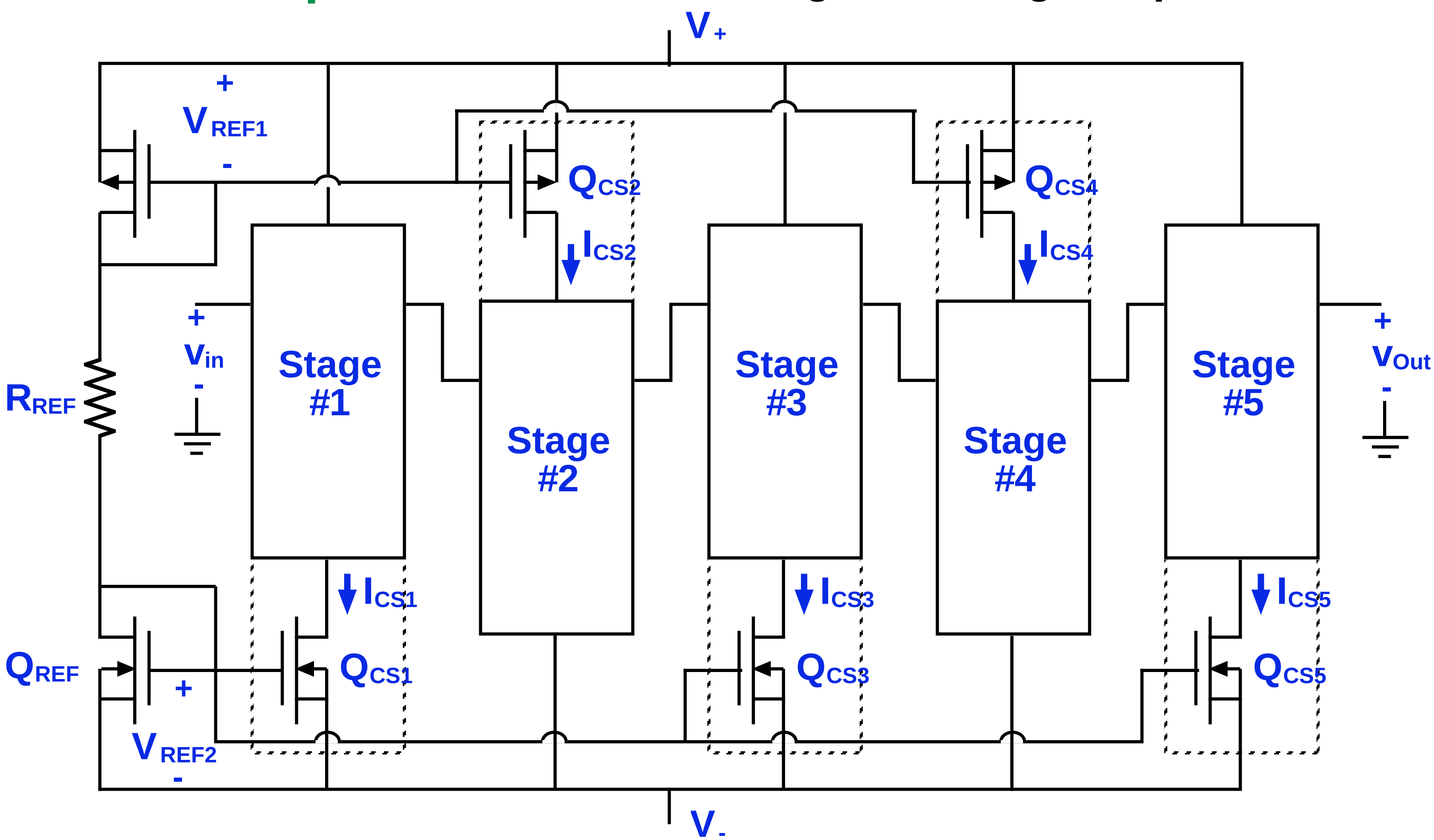


Norton Output

Two-ports can simplify the analysis and design of multi-stage amplifiers:

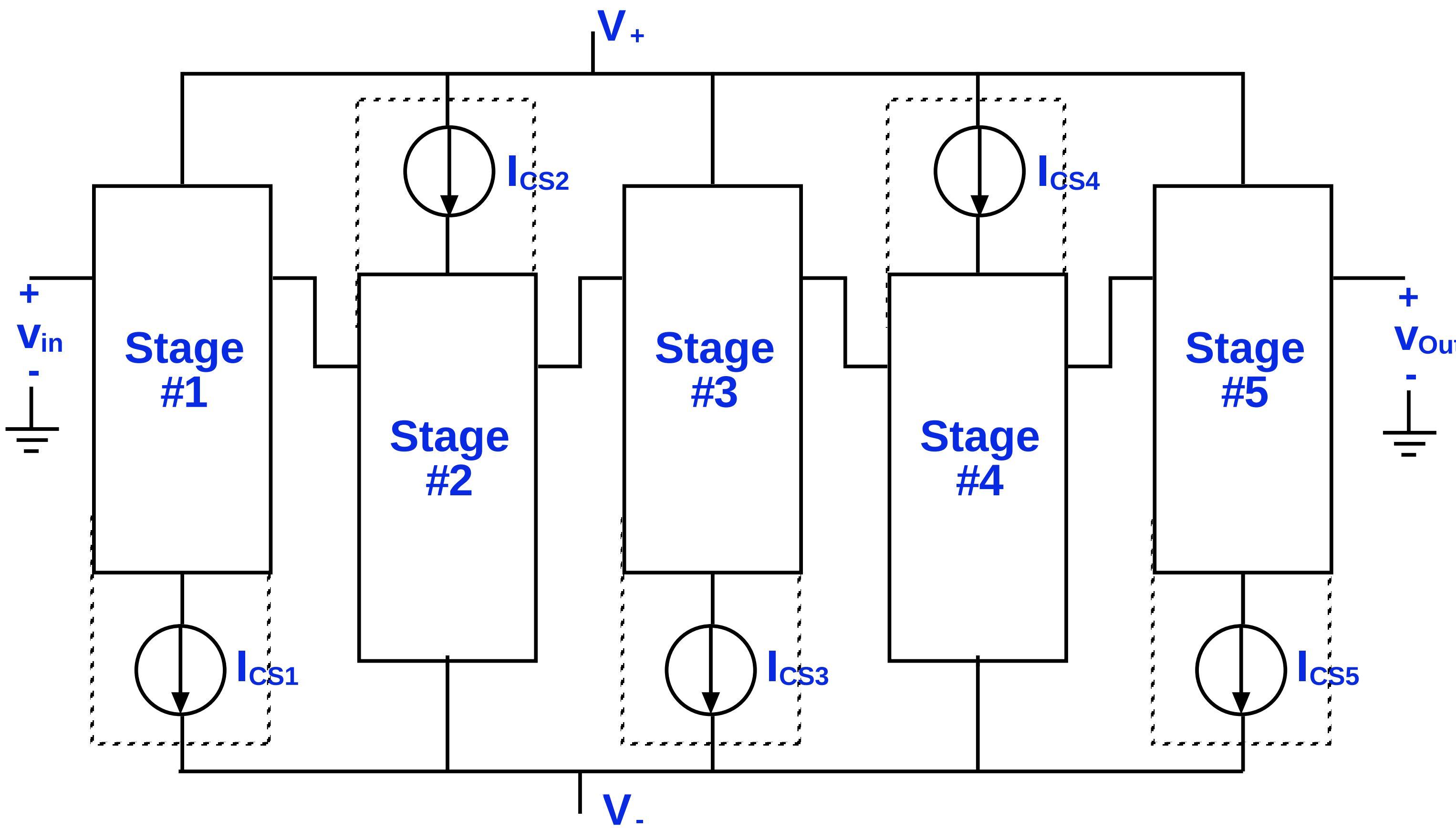


Linear amplifier basics: Biasing multi-stage amplifiers



⇒ The current mirror voltage reference method can be extended to bias multiple stages, and one reference chain can be used to provide V_{REF} to all the sources and sinks in an amplifier.

Linear amplifier basics: Biasing multi-stage amplifiers. cont.



When looking at a complex circuit schematic it is useful to identify the voltage reference chain and the biasing transistors and replace them all by current source symbols.

This can reduce the apparent complexity dramatically.

Lecture 17 - Linear Amplifier Basics; Biasing - Summary

- **Biasing transistors**

  Current source biasing: current sources to establish stable bias pts.
  large signals models are used in this analysis

  Transistors as current sources: great as long as stay in FAR

  Current mirror current sources and sinks: it takes one to know one

- **Mid-band analysis**

  Biasing capacitors: short circuits above ω_{LO}

  Device capacitors: open circuits below ω_{HI}

  Midband: $\omega_{LO} < \omega < \omega_{HI}$

- **Linear amplifiers**

  Performance metrics: gains (voltage, current, power)

  $A_v = v_{out}/v_{in}$, $A_i = i_{out}/i_{in}$, $A_{power} = v_{out}i_{out}/v_{in}i_{in}$

  input and output resistances

  $r_{in} = v_{in}/i_{in}$, $r_{out} = v_{test}/i_{test}$ with $v_{in} = 0$

  dc power dissipation: $(V_+ - V_-)(\Sigma I_{BIAS}\text{'s})$

  bandwidth **(We'll save bandwidth for later - Lecs. 23/24)**

  Multi-stage amplifiers: two port models and analysis
  current mirror biasing of multiple stages

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