MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 MICROELECTRONIC DEVICES AND CIRCUITS

Answers to Exam 2 - Fall 2009

Problem 1: Graded by Prof. Fonstad

a) i) Applying $v_{GS} > V_T$ to an n-channel MOSFET accumulates additional holes at the interface. The additional amount of interface charge is $-WLC_{ox}^*(v_{GS} - V_T) = -5 \times 10^{-4} \times 2 \times 10^{-5} \times 10^{-8} \times 1 = 10^{-16}$ Coul.

ii) The additional holes come from the p-type bulk region.

iii) Applying $v_{GS} < V_{FB}$ to an n-channel MOSFET increases the number of inversion layer electrons at the interface. The additional charge is $-WLC_{ox}^*(v_{GS} - V_{FB}) = 5 \times 10^{-4} \times 2 \times 10^{-5} \times 10^{-8} \times 1 = 10^{-16}$ Coul.

iv) The additional electrons come from the n-type source and drain regions.

b) i) One of the n+ regions (source or drain) is the emitter, the other n+ region is the collector, and the base is the p-region, or substrate. To bias an npn BJT in its forward active region requires $V_{CE} \geq 0.2$ V and $V_{BE} \approx 0.6$ to 0.7 V. Saying both had to be greater than zero was accepted and earned most of the points.

ii) The forward current gain, β_F, is low because a large fraction of the electrons injected across the emitter-base diode into the p-region are directed vertically and not laterally toward the collector.

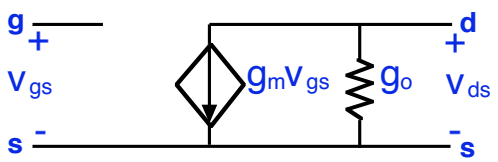
The early voltage is low, and thus there is a significant amount of base width modulation, because the collector is more heavily doped than the base, meaning that the depletion region at the collector-base junction extends primarily into the base side of the junction.

iii) Adding a heavily doped p-type region under the n+ regions reduces the vertical injection of electrons across the emitter-base junction and the junction current is now predominantly electrons flowing laterally across the junction and toward the relatively close collector. This makes β_F much larger.

c) i) Doing a Taylor's Series expansion about Q, and isolating the small signal terms:

$$i_d = (di_D/dv_{GS})\,|_Q\, v_{gs} + (di_D/dv_{DS})\,|_Q\, v_{ds}$$
$$= (W/L)\,\mu_e\,[C_{ox}^*\,V_{DS}\,v_{gs} + (C_{ox}^*\,V_{GS} + \alpha)\,v_{ds}]$$

ii) The small signal linear equivalent circuit is:

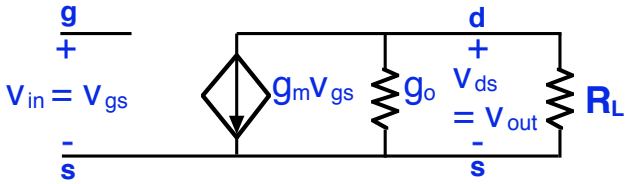


with $g_m = (W/L)\,\mu_e\,C_{ox}^*\,V_{DS}$ and $g_o = (W/L)\,\mu_e\,(C_{ox}^*\,V_{GS} + \alpha)$

iii) To find R_L we first find $I_D = 10^{-7}\,(10\,V_{GS} + 1)\,V_{DS}$ with $V_{GS} = 1$ V and $V_{DS} = 1.5$ V, or $I_D = 1.65 \times 10^{-6}$ Amps. The voltage drop across R_L must be 1.5 V, so

$$R_L = 1.5/(1.65 \times 10^{-6}) \approx 900{,}000 \text{ Ohms}$$

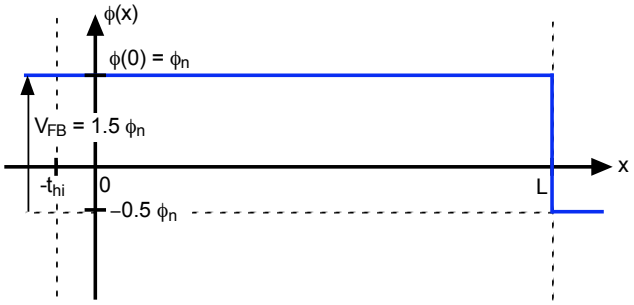
We can now use this result and our linear equivalent circuit to draw the linear equivalent circuit for the full circuit, and from that we find the voltage gain:



We find $g_m = 1.5 \times 10^{-6}$ mho and $g_o = 1.1 \times 10^{-6}$ mho, and using the R_L above we have $1/R_L = G_L = 1.1 \times 10^{-6}$ mho. Thus, $A_v = v_{out}/v_{in} = -g_m/(g_o+G_L) \approx -0.7$.

Problem 2: Graded by Prof. Weinstein

a) In flatband there is no depletion region, $\phi(0) = \phi_n$, and there is no voltage drop across the dielectric.



As indicated in the figure, $V_{FB} = 1.5\ \phi_n$.

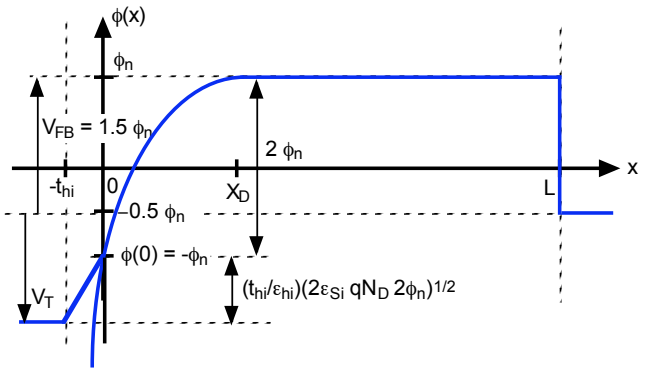
b) At flatband the hole and electron populations are the same as they are in the bulk of the semiconductor. Thus, $n(x = 0^+) = N_D$, and $p(x = 0^+) = n_i^2/N_D$.

c) At the onset of threshold $\phi(0) = -\phi_n$, the depletion region accommodates a change in potential of $2\ \phi_n$ and thus $X_D = [2\varepsilon_{Si}\ (2\ \phi_n)/qN_D]^{1/2}$. The potential drop across the dielectric $qN_DX_Dt_{hi}/\varepsilon_{hi}$, and $V_T - V_{FB} = -2\ \phi_n - (t_{hi}/\varepsilon_{hi})[2\varepsilon_{Si}\ (2\ \phi_n)\ qN_D]^{1/2}$.

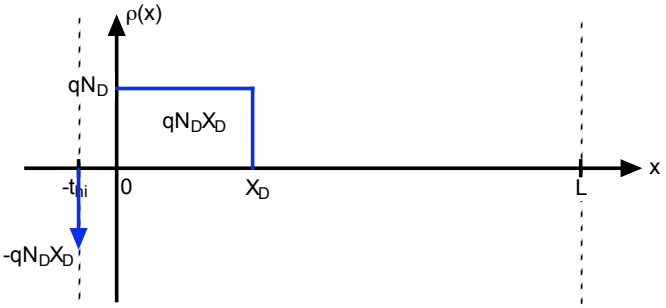
With these results, we find $V_T = V_{FB} - 2\ \phi_n - (t_{hi}/\varepsilon_{hi})[2\varepsilon_{Si}\ (2\ \phi_n)\ qN_D]^{1/2}$

$= -0.5\ \phi_n - (t_{hi}/\varepsilon_{hi})[2\varepsilon_{Si}\ (2\ \phi_n)\ qN_D]^{1/2}$

The electrostatic potential profile at the onset of inversion:



The net charge distribution at the onset of inversion:



d) At the onset of inversion, the hole density at the interface is N_D, i.e. $p(x = 0^+) = N_D$, and $n(x = 0^+) = n_i^2/N_D$.

e) If there is a net sheet charge density, σ_i, at the interface, then at flatband there is a net sheet charge density, $-\sigma_i$, on the gate, and no other charge in semiconductor up to the interface. The voltage drop across the gate dielectric is $\sigma_i(t_{hi}/\varepsilon_{hi})$, and the flatband voltage must be more negative by this amount, $\Delta V_{FB} = -\sigma_i(t_{hi}/\varepsilon_{hi})$. The threshold voltage will be more negative by this same amount: $\Delta V_T = -\sigma_i(t_{hi}/\varepsilon_{hi})$.

f) With an additional dielectric layer under the gate, there is additional voltage drop across the insulator for the same charge on the gate: ΔV (w.o. SiO_2) $= Q_G(t_{hi}/\varepsilon_{hi})$ and ΔV (w. SiO_2) $= Q_G(t_{hi}/\varepsilon_{hi}) + Q_G(t_{ox}/\varepsilon_{ox})$. $C_G = Q_G/\Delta V = 1/(t_{hi}/\varepsilon_{hi} + t_{ox}/\varepsilon_{ox}) = \varepsilon_{hi}/2t_{hi}$. Thus C_G(w. SiO_2)/ C_G(w.o. SiO_2) = ½.

Problem 3: Graded by Prof. Palacios

a) $I_{D,sat} = (W_{min}/2L_{min})\mu_e(\varepsilon_{ox}/t_{ox})(V_{GS} - V_T)^2[1+\lambda_n(V_{DS}-V_{DS,sat})]$

$= [135/(2 \times 35)] \times 500 \times (3.5 \times 10^{-13}/10^{-7})\ (0.6)^2\ (1+0.001(1-0.4)) \approx 1.2$ mA

b) $r_o = 1/g_o = 1/\lambda_n I_D = 1/(10^{-3} \times 1.2 \times 10^{-3}) = 10^{-6}/1.2 \approx 800{,}000$ Ohms

c)

V_{IN1}	V_{IN2}	V_{OUT}
0 V	0 V	1 V
0 V	1 V	1 V
1 V	0 V	1 V
1 V	1 V	0 V

d) $W_{n,\,Inverter} = 1\ W_{min}$ and $W_{p,\,Inverter} = (\mu_e/\mu_h)\ W_{n,\,Inverter} = (500/200)\ W_{min} = 2.5\ W_{min}$

e) We want the n-MOSFETs to each be minimum length since the effective length will be the sum of the lengths of two n-MOSFETs: $L_{n,NAND} = 1\ L_{min}$. and $L_{n,Eff} = 2\ L_{min}$. To minimize the delay, we will require the same current capability as in a standard inverter. To achieve this with an effective gate length $L_{n,Eff} = 2\ L_{min}$, the width needs to be $W_{n,NAND} = 2\ W_{min}$.

As the current capability of the n-MOS branch is the same as in an inverter, the p-MOS branch can be sized as in the inverter in question d). Thus $C_{IN,NAND} = 2.5W_{min}L_{min} + 2W_{min}L_{min} = 4.5\ W_{min}L_{min}$. $C_{IN,Inverter} = W_{min}L_{min} + 2.5\ W_{min}L_{min} = 3.5\ W_{min}L_{min}$, so $C_{IN,NAND} = 1.29\ C_{IN,Inverter}$.

f) The question speaks of inverter equivalents. The inverters have 15nA leakage if their output is high (n-MOS off), and 37.5 nA leakage if their output is low (p-MOS, which is 2.5 x as wide, off) so the static power dissipation is 15 nA/gate x 1 V x 10^9 gates + 37.5 nA/gate x 1 V x 10^9 gates = 47.5 Watts!

If you did the problem assuming 10^9 NAND gates, then the output is low, we have subthreshold current coming from each one of the two p-MOSFETs, which are connected in parallel. Therefore, the power dissipation is: 2 transistors/gate x 15 nA/transistor x 1 V x (1×10^9) gates = 30 Watts. When the output is high, the leakage current is due to the subthreshold current through the n-MOSFETs, which are connected in series and the current is dominated by one of them (i.e. they share the same current). Thus, the power dissipation in this state is: 1 transistor/gate x 15 nA/transistor x 1 V x (1×10^9) gates = 15 Watts. By adding the two contributions, the total dissipated power is: 30 W + 15W = 45 W

g) i) $E_{ave} = 1\text{ V}/(35 \times 10^{-7}\text{ cm}) \approx 3 \times 10^5\text{ V/cm}$

ii) The average sheet charge density is $q_n^* = C_{ox}^*(v_{GS} - V_T) = 0.6\ (\varepsilon_{ox}/t_{ox}) = 0.6 \times 3.5 \times 10^{-6} = 2.1 \times 10^{-6}\text{ coul/cm}^2$. The current, $i_D = W\, q_n^*\, s_{ch,ave}$. Assuming $i_D = 250\ \mu\text{A}$, we have: $s_{ch,ave} = i_D/(W\, q_n^*) = 2.5 \times 10^{-4}/(1.35 \times 10^{-5} \times 2.1 \times 10^{-6}) \approx 0.88 \times 10^7\text{ cm/s}$.

Assuming $i_D = 1.2$ mA as found in part (a), we find: $s_{ch,ave} \approx 4.2 \times 10^7\text{ cm/s}$.

iii) The current is almost 5 times smaller than the low field constant mobility model predicts because the velocity saturates at just under 10^7 V/cm.

Exam Statistics

Average/Standard deviation:	Problem 1	21.5	5.3
	Problem 2	19.2	7.6
	Problem 3	25.1	5.5
	Total	65.8	14.9

Class median: 65

Distribution to nearest 5:

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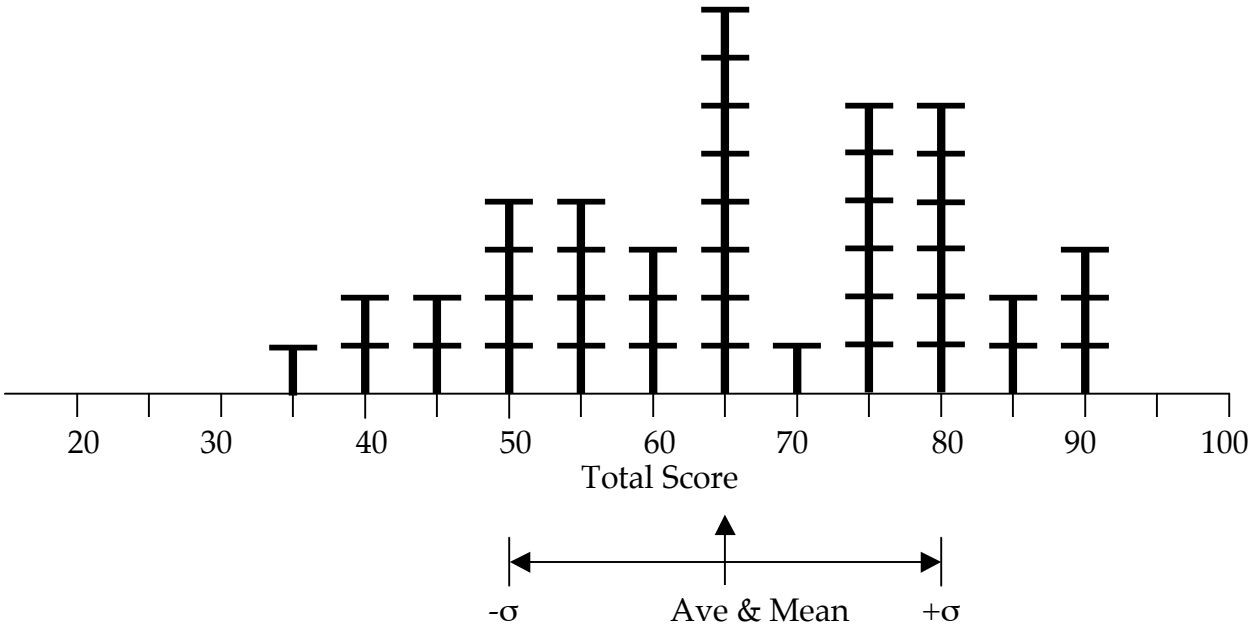

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