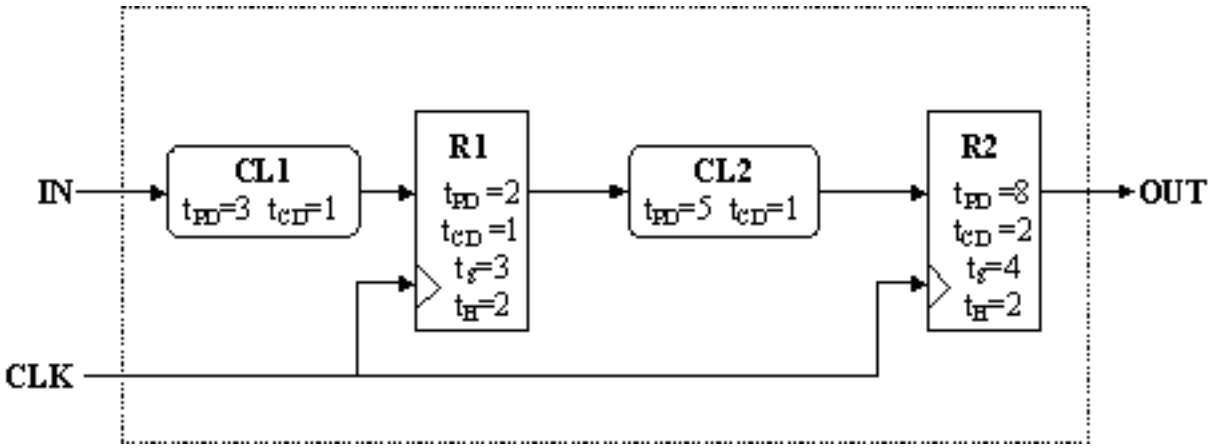
6.004 Computation Structures
Spring 2009

Sequential logic and memory components

Problem 1. Consider the following diagram of a simple sequential circuit:

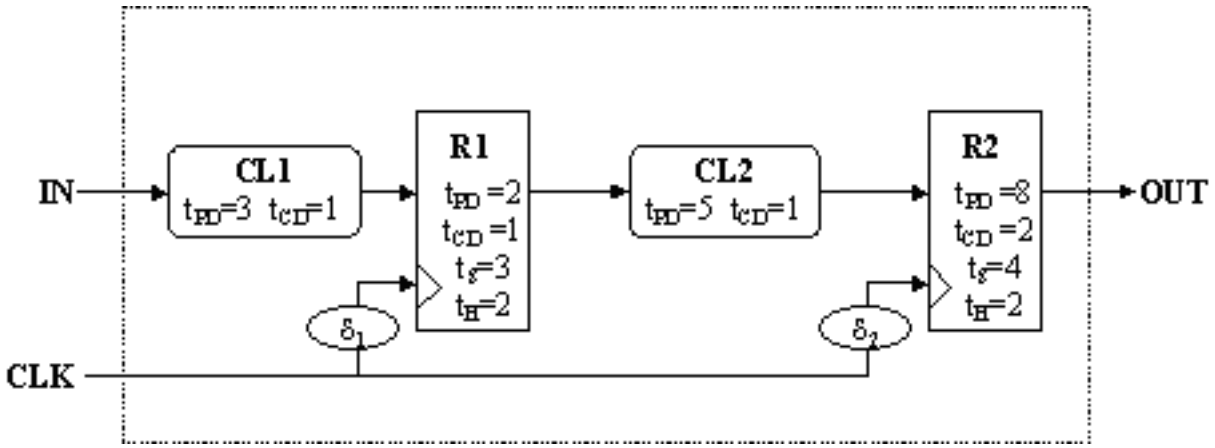


The components labeled CL1 and CL2 are combinational; R1 and R2 are edge-triggered flip flops. Timing parameters for each component are as noted.

A. ★ Write the timing specifications (tS, tH, tCD, tPD, tCLK) for the system as a whole using the timing specifications for the internal components that are given in the figure.

B. ★ Suppose you had available a faster version of CL2 having a propagation delay of 3 and a contamination delay of zero. Could you substitute the faster CL2 for the one shown in the diagram? Explain.

C. We've been treating wires as idealized components that introduce no delay of their own. In the real world, wires have resistance, capacitance and inductance that will cause different frequencies to propagate along the wire at different rates. This means that wires will delay the arrival of sharp rising and falling transitions (which you'll remember from Fourier analysis have signal components at many different frequencies). This effect is particularly bothersome in connection with clock signals since the clock may arrive at separate parts of the circuit at slightly different times. This difference in arrival times of the clock is called **clock skew**, which we'll model in our simple circuit above as explicit delays along each clock path:



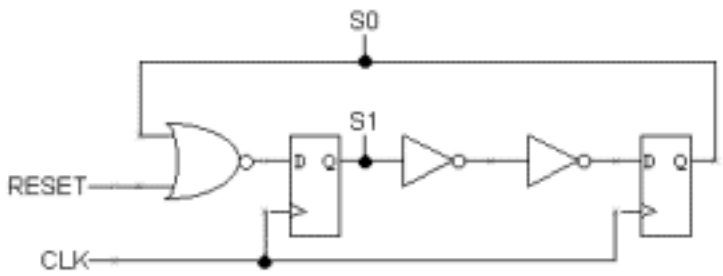
D. Rewrite the timing specifications for the system as a whole taking into account d1 and d2. Don't make any assumption about the relative sizes of the two delays.

E. The relative clock skew (d2 - d1) between two registers connected in a "pipeline" - where the output of the first register is connected, usually through logic, to the input of the second register - can also affect the design of a circuit. Explain how relative clock skew affects the maximum clock frequency of the circuit shown above. Remember that the relative skew might be positive or negative.

F. [Why clock skew keeps integrated circuit designers awake at night.] If d2 > d1, the circuit shown above will not operate correctly. Explain why. Will changing the frequency of CLK solve the problem? Why or why not?

G. Suggest a way for the designer to change his circuit to guarantee correct operation given an upper bound, tskew > abs(d2 - d1), on the maximum relative clock skew. Assume that the timing parameters of the registers cannot be adjusted.

Problem 2. The following circuit diagram implements a sequential circuit with two state bits, S0 and S1:



inverter: t_{CD}=1ns, t_{PD}=2ns
nor2: t_{CD}=1.5ns, t_{PD}=2ns
D register: t_{CD}=0ns, t_{PD}=2ns, t_H=1ns, t_S=3ns

A. ★ What is the smallest clock period for which the circuit still operates correctly?

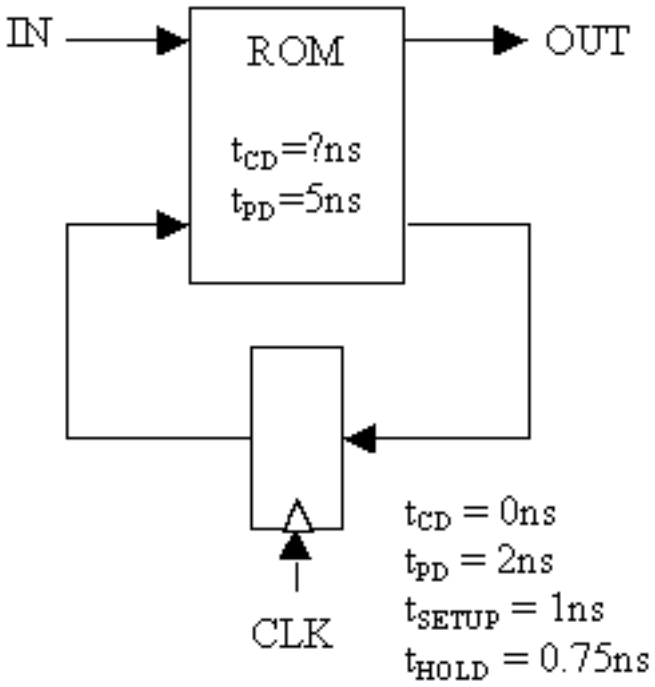
B. ★ A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed.

C. ★ When the RESET signal is set to "1" for several cycles, what values are S0 and S1 set to?

D. ★ Assuming the RESET signal has been set to "0" and will stay that way, what is the state following S0=1 and S1=1?

E. ★ Now suppose there is *skew* in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1ns before it arrives at the right register. What is the smallest clock period for which the circuit still operates correctly?

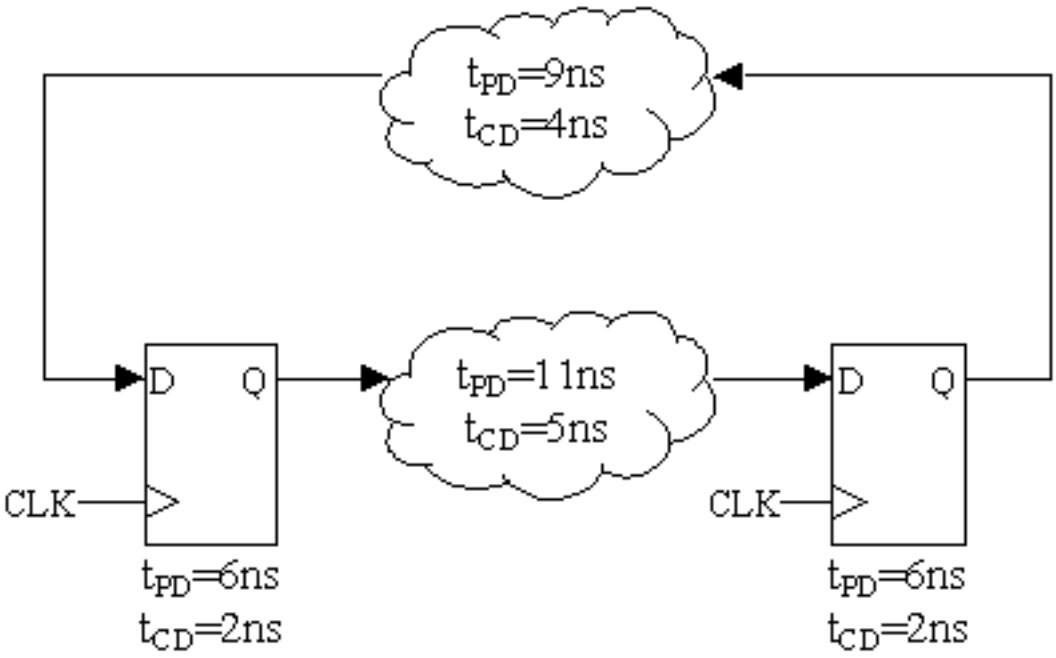
Problem 3. A possible implementation of a sequential circuit with one input and one output is shown below.



A. What is the smallest value for the ROM's contamination delay that ensures the necessary timing specifications are met?

B. Assume that the ROM's tCD = 3ns. What is the smallest clock period that ensures that the necessary timing specifications are met.

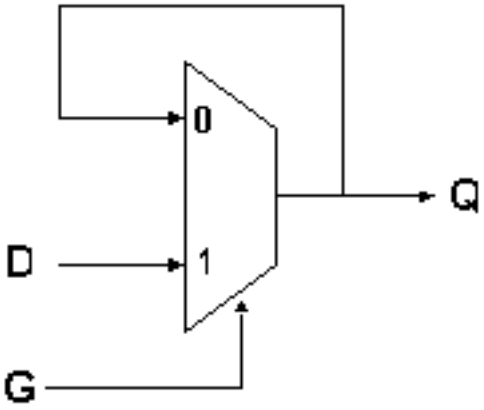
The following schematic has two flip-flops and two blocks of combinational logic with the indicated timing specifications. Assume that the flip-flops are identical and that the clock has zero rise and fall time.



C. Assuming that the clock period is 25ns, what is the maximum setup time for the flip-flops for which this circuit will operate correctly?

D. Assuming that the clock period is 25ns, what is the maximum hold time for the flip-flops for which this circuit will operate correctly?

Problem 4. In lecture, you saw a static latch constructed from a 2-input lenient MUX as shown in the diagram below.



Recall that the MUX selects the Q output when G=0, and the D input when G=1. The plan is that when G=1, the Q output will follow D after a short delay; when G=0, the current Q output will be "latched" via the feedback path. In this problem we explore assumptions necessary to construct an informal proof that the latch behaves as proposed. Assume, in each of the following, that the MUX is a well-behaved lenient combinational device with a propagation delay of tpd.

Recall that the lenience of the MUX allows us to assume that if any two of its inputs sufficient to determine its output are stable and valid for at least tpd, then the MUX output will be stable and valid.

A. Specify constraints on the two data inputs of the MUX sufficient to guarantee that its output will be stable and valid independently of the value on the select input.

B. Specify constraints on a single data input and the select input of the MUX sufficient to guarantee stable and valid output independently of the value on the remaining data input.

C. Now we explore the scenario where G=1 and D has been stable and valid for ts seconds prior to a 1-to-0 transition on G, and remains stable and valid until th seconds after the transition on G. Our goal is to establish that, for sufficiently large values of ts and th, the latch behaves as advertised.

   Consider the initial interval in the above scenario where G=1. At what point is Q=D guaranteed? Explain why in a sentence or two.

D. Explain why, for sufficiently large values of tS the output Q remains stable despite invalid voltages on G. What is the setup time required to guarantee output validity during the transition on G?

E. Now assume that D changes tH seconds after the transition on G. Explain why, for a sufficiently large value of tH, the Q output will remain stable independently of D.

F. Identify which of your previous answers is dependent on the MUX being lenient, giving a single-sentence description of the dependence.

G. Does the operation of the above latch depend on the contamination delay of the MUX? Explain.

H. Your analysis has established setup and hold time requirements necessary to guarantee proper operation of the latch. Suppose, in the above scenario, the setup or hold time requirement is violated? What can you say about the value on Q?