All right. Let's get started.

I guess this watch is a couple minutes fast.

First a quick announcement. In case you have forgotten, your lab notebooks are due tomorrow with the post-lab exercises for the first lab. OK, so I am going to continue with amplifiers today. And to just give you a sense of where we headed, we have this five lecture sequence covering different aspects of amplifiers with dependent sources and showed how we could build an amplifier with it on Tuesday. Today I am going to show you a real device that implements a dependent source.

And then next Tuesday we will talk about analysis of an amplifier. Wednesday is our quiz.

Thursday and the Tuesday after that we then talk about small signal analysis and small signal use of the amplifier.

Today we will talk about the MOSFET amplifier.

So let's start with a quick review.

And in the last lecture, I showed you that I could build a amplifier using a dependent source.

And a dependent source worked as follows.

Let's say I had a circuit and I connected a dependent source into the circuit. Let's say in this example I have a current source. So this is some circuit.

And the current i is a function of some parameter in the circuit. That's why this is a dependent source. This is a dependent current source. So it could be that I have some element inside. And I measure, I sample the voltage across the element or between any two points in the circuit. And, in this little example here, this current could be dependent on that voltage.

So notice that although I showed you the two terminals of the dependent source that carried a current, there is another implicit port, another implicit terminal there. And that terminal there is called the "control port" of the dependent source at which I apply a voltage or current that will control the value of the current source. As a quick aside.

There is a small glitch with the tools in your tool chest.

We talked about the superposition technique where you were taught to turn on one source at a time, for a linear circuit one source at a time, and then sum up the responses to all the sources acting one at a time.

Well, what do you do about dependent sources?

A dependent source is a source. And we have to modify the superposition statement just a little bit.

And for details you can look at Section 3.5.1 of your course notes on the details and some examples on how to do this.

So the approach is very simple, actually.

The approach is, for the purpose of superposition, to not treat your dependent source as sources that you turn on and turn off.

So what you do is when you do superposition with dependent sources simply leave all your dependent sources in the circuit. Just leave them in there and turn on and off only your independent sources.

So look at the response of the circuit by turning on your independent sources one at a time and summing up the responses. And your dependent sources stay within the circuit and simply analyze them as you do anything else. So essentially what it says is that just be a little cautious when you have dependent sources, but the basic method applies almost without any change.

The readings for today's lecture are Section 7.3 to 7.6.

So since we are going to build up on the dependent source amplifier, let me start with a quick review of that amplifier.

We built our amplifier as follows.

We connected our dependent source in the following manner.

And the current through the dependent source in the example we took was related to an input voltage vI.

So some voltage vI. And so these two were the control port of the dependent source and a vI was applied there. And I showed you a simple amplifier built with a dependent source that behaved in this manner. And again I will keep reminding you, just remember that the dependent source is actually this box here, the control port and the output port. And commonly we don't explicitly show the control port for those dependent sources for which the control port does not have any other affect on the circuit, like it doesn't draw any current or things like that.

So in this particular example we said that this behaved in the following manner for vI greater than or equal to 1 volt and iD was zero otherwise.

So we can analyze the circuit to figure out what vO is going to look like. And a simple application of KVL at this loop here, again, you know, when I say this loop here, I am pointing at something here. That is the VS source that is implicitly across these two nodes.

Again, this is a shorthand notation where this little up arrow here implies that I have a voltage source connected between these two terminals here. And so there is a loop here that involves VS. So Vo is simply VS minus the drop across this resistor. So it's VS minus the drop across this resistor gives me vO.

And the drop across the resistor is simply iD RL.

iD is the current here and that's the drop across the resistor. And I could get the explicit relationship of vO versus vI by substituting for iD as vI minus one all squared. So vO relates to vI in the following manner. Nothing new so far.

I have pretty much reviewed what we did the last time.

Here is where we take our next step forward with some new material. Up to now I have talked as a theoretician would where I said just imagine that you had spherical cow or something like that.

Here I just asked you to imagine this ideal dependent source, control port and an output port, and it behaved in this manner. So as a next step what I would like to do is show you a practical dependent source which turns out to be a little bit more complicated than this idealized dependent source that I showed you in many dimensions.

Real life tends to impose a bunch of practical constraints on you, and we will look at those in a second.

If I could find a dependent source that looked like this -- We had a control port A prime and output port B prime.

And I looked at some examples where the current through the dependent current source was some function of the input voltage. This is a "voltage controlled current source". What I am going to do is talk about a device that can give me this behavior or some close approximation to it. It turns out that under certain conditions the MOSFET that you have already looked at behaves in this manner. The MOSFET that you've seen sort of behaves like this. And let me show you under what conditions the MOSFET behaves in that manner.

Let me create some room for myself.

Notice that I need a control port, needed an output port.

And I am going to view my MOSFET in a slightly different manner than you have seen before.

I draw these two terminals here.

And this was a three terminal MOSFET.

This was my drain, my gate and my source terminal.

It was a three terminal device, but what I do is I view the MOSFET slightly differently. I will just use this terminal to be common across both the gate and the drain.

And so this voltage here is vGS.

I am just using the source port, the source terminal along with the gate as a terminal pair.

I am using the same source along with the drain as another terminal pair. So I have a vDS out there and I have some current iDS that flows out here.

Notice that when I view the MOSFET in this manner I have accomplished my first step, which is I seem to have a box which has a port here and a port here.

And I also explained to you that a MOSFET behaves in a particular manner. For one, the output port behaved as an open circuit under certain conditions when -- This was vGS, G, drain and source.

When vGS was less than a threshold voltage VT this MOSFET had an equivalent circuit that looked like this.

So when vGS was less than some threshold voltage VT then there was an open circuit between the drain and the source.

And you saw this before. So far nothing new here.

However, when vGS is greater than or equal to VT -- vGS was greater than VT. The MOSFET behavior we looked at earlier showed that this behaved either like a short circuit in the simplest form or in a slightly more detailed form it behaved like a resistor. We call that the SR model of the MOSFET. So when vGS was greater than VT we said that a simple way to approximate MOSFET behavior was to view this as a resistor connected between the drain and the source. That was our SR model use of the MOSFET. It turns out that we kind of lied. We were sort of looking at the MOSFET in a really funny way. And I shone the light on the MOSFET in a really, really clever way.

Well, I shouldn't say clever. A really, really tricky way.

And tricked you into believing that it was just a resistor.

And we constrained how you use the MOSFET.

So that behavior was indeed a resistive behavior.

But it turns out that in real life the behavior of the MOSFET between the drain and the source terminals is much more complicated than the limited form in which you saw it.

So today what I am going to do is take the wraps off the complete MOSFET and show you its full behavior in all its gory glory. And I will spend a bit of time on that to clearly emphasize under what conditions the MOSFET behaves like a resistor, as you saw when you did digital circuits, or behaves differently in other domains of use.

Let me pause for a second and leave this space blank here.

And let's do some investigations.

Let me leave this here. I won't draw in anything yet.

You will figure out what it looks like yourselves under certain conditions. What I will do next is apply some voltages on a MOSFET and observe the current versus vDS behavior and plot that on a scope and take a look at it.

What I am going to do -- -- is figure out what iDS looks like for -- Remember iG into the gate for 6.002 is always going to be zero. In much more detailed analyses of the MOSFET, in future courses you may see slightly more complex behavior. But as far as we are concerned it is an open circuit looking into the gate.

So I am going to apply a vGS across the MOSFET, apply a vDS across the MOSFET and plot iDS versus vDS.

First let me show you what you already know.

What you already know -- This is vDS. I will just keep doing as much as I can of what you already know.

And then when I do some new stuff I will tell you explicitly. You've seen this before.

The MOSFET behaves like an open circuit when vGS less than VT.

That is when vG is less than a threshold voltage VT, I have zero current flowing through the MOSFET.

And when vGS was greater than VT then the S model of the MOSFET the switch model simply said that look, we can model the D2S as a short circuit.

You saw this in your labs and you saw that it was a very, very small resistance between the drain and the source and it kind of looked like a short circuit.

But then we said well, that's not quite it.

There is some resistance. And so we said a slightly more accurate model would have this line droop a little bit to imply that there was some resistance R_on between the drain and the source, so vDS iDS. So this was when vGS less than VT and vGS greater than or equal to VT.

I have some resistance. And that showed me a straight line kind of like behavior. And I showed you that behavior.

So far absolutely nothing new. Now what I have plotted there for you is that behavior. Up here notice that this is the vDS axis, this is the iDS axis. I am plotting iDS versus vDS.

And when vGS -- The gate voltage is more than a threshold, notice that I see what looks like something more or less like a straight line. And this is a straight line with some slope, more or less a straight line implying resistive behavior. And we also had some fun and games here. We said hey, what if I turn vGS off? Boom.

That would be my iDS of zero implying that the MOSFET behaved like an open circuit between the drain and the source.

I applied a positive vGS more than VT and it began to look like a resistor. Open circuit, resistor, open circuit, resistor, OK?

Up until now nothing new. So you shouldn't have learned anything at all that is new until now in today's lecture.

Now watch. What I am going to do is, as I said, I kind of lied all this time and I just showed you this behavior. And what I have been doing all along is very carefully using a very small value of vDS.

Notice it's a small values of vDS.

I haven't told you what it looks like as vDS increases.

Well, let's go try it out. We have a scope here.

We have the MOSFET here. Now, I am not sure what is going to happen now. You may see smoke or have an explosion, who knows what? But look up there for a second.

I am just going to increase vDS and you can figure out what happens for yourselves. I increase vDS.

Whoa, what a liar. Agarwal is a liar.

I have been kind of tricking you.

I have been putting -- Covering up all this part here and showing you just this region of the curve for small values

of vDS. But as I increase vDS this is nothing that looks even close to that of resistive behavior.

So what's happening here? What's happening is that as I increase my vDS the iDS curve tails off and saturates at some value of current. Notice it saturates at some value of current. And so I am going to look at this region of behavior. Notice that what we have looked at so far was the behavior for small vDS.

It kind of looks resistive. But when I pump up the vDS, really whack this node really hard with a much larger vDS the guy says, oh, I give up.

And the current saturates out and flattens out and holds the value steady at some value. So what's that behavior look like? What is my horizontal line above the X axis in terms of V I elements?

What is that behavior like? Current source, exactly. So this is current source like behavior. And so let me start by drawing you a little model and explaining it in more detail.

What happens is that under certain conditions, and the conditions are the following, when vDS, that is my drain to source voltage is greater than or equal to vGS minus VT. When my drain voltage goes above vGS minus VT, so if vGS is 3 volts and if VT is 1 volt, then if vDS goes above 2 volts, if I am hammering the drain of the MOSFET with a higher voltage then this guy says I give up, can't show you nice restive behavior, and the current saturates out and it doesn't allow you draw any more current than a maximum value.

And that's the current source behavior.

This one behaves like a current source.

And the current iDS is given by the following expression.

The current is given by iDS is equal to a constant K divide by two times (vGS-VT) all squared. Kind of reminiscent of the carefully chosen dependent source example, just that this one here is VT. This model, which applies when vGS is greater than VT, the MOSFET has to be on and the drain to source voltage in the MOSFET must be larger than some value, and that value is vGS minus VT then this guy begins to behave like a current source. This model of the MOSFET is called the "switch current source model".

So in the region of the MOSFET characteristics where vGS is greater than VT and the drain to source voltage is larger than vGS minus VT, the MOSFET behaved like a current source between its drain and source terminals.

And in that part we model the MOSFET as a current source.

And so not surprisingly that part of the model is called the SCS model in contrast with the SR model where we had

a resistor. Again, remember, this is not meant to be conflicting.

It is not like gee, how can the MOSFET look like a resistor, and then suddenly what happens it becomes a current source. Well, the two regions are different. It is not that it is behaving as a current source for the same parameters, no.

When vDS is less than this right-hand side it does behave resistive. The SR model applies.

But increase vDS beyond a point, the current saturates and the SCS applies like so. So let's draw.

The SCS behavior can be drawn here vDS and iDS.

As I mentioned to you, for small values of vDS, let's say I pick some value of vGS, let's say vGS3, some value vGS, it is going to look like a resistor until vDS becomes equal to vGS3 minus VT.

And after that it saturates out and begins to look like a current source. And this point is where vDS becomes equal to vGS minus VT. And this way is when this equal sign becomes a greater than sign, vDS becomes larger then I move into this part of the curve.

Similarly, for various other values of vGS it will look like this -- -- and so on. And it behaved like an open circuit as before when vGS less than VT.

When vGS less than VT it is still behaving like an open circuit. And so as I increase my vGS, provided I keep my vDS greater than vGS minus VT, I get current source like behavior.

And notice that this is increasing vGS.

I have purposely drawn these curves at greater distances from each other to imply that it is a nonlinear relationship in that if I increase vGS by some amount, the increase in vDS is related to the square of vGS. It is vGS minus VT all squared.

So I get a family of curves of that look like this.

And this is in the region of operation where vDS equals vGS minus VT. And this applies in this regime where vDS less than vGS minus VT.

This region of operation is called, as you might expect, the "saturation region".

We say the MOSFET has been hammered, the MOSFET has been walloped, the MOSFET is in saturation.

So the MOSFET is in saturation. This region, corresponding to this, is called the triode region.

This is really very simple. All we are doing is saying that when vDS is increased beyond a certain limit, given my vGS minus VT, the MOSFET begins to behave like a current source. It cannot draw any more current. It limits the current to a given value like a current source.

But on the left-hand side of this it behaves in a resistive manner. So what I would like to do is -- What I will do is, we've plotted for you, for the MOSFET, all its characteristics in its full glory for a whole bunch of values of vGS and a whole bunch of values of vDS. And let me stare at those curves with you for a few seconds and walk you through them. So what do I have here?

One of these curves corresponds to a given value of vGS.

This may be vGS equals 2 volts. This is vDS, the drain to source voltage, and this is the current.

So focus on this curve for now. In the beginning I hid the right-hand side behavior from you and showed you just the resistive behavior out here. When I increase vDS to be much larger the curve saturated and I got the saturation region operation of the MOSFET. And notice as I increase my value of vGS the saturation current also increases according to a square law behavior. So these are the entire curves of the MOSFET. Finally the truth comes out.

And notice that when vDS is less than vGS minus VT, I have more or less resistive behavior.

But when vDS is greater than vGS minus VT I get current source like behavior. So one question you may ask is when do I use one model or the other?

When do I use the SR model and when do I use the SCS model?

If you want to do a real detailed analysis then you can use the SR model when vDS is less than vGS minus VT.

And you would use this model when vDS is greater than or equal to vGS minus VT. That is simple enough.

In 6.002, to eliminate confusion we constrain how we look at things a little bit more stringently.

And what we do is that for our entire digital analysis, for the entire digital world we focus on the SR model.

And I will tell you why in a second.

So for all digital circuits, invertors, look at power of invertors, look at delay, a bunch of other things, we will be using the SR model in 6.002.

And I will tell you why in a second.

And for analog -- That is for amplifier designs and situations like that, we will be operating the MOSFET in a saturation region. And I will talk about that in a second. What I am saying here is that in 6.002, when we do analog designs, we are going to discipline ourselves to using the MOSFET only in this region.

We are going to constrain ourselves to play in only this region of the playground where vDS is quite large.

Why? Because I am asking you to.

I am saying let's play in that part of the playground and keep your vDS high. And so the MOSFET is going to be operating somewhere in here. So we can apply just the SCS model, just the current source behavior in that region.

There is another important reason, which I will get to in a second. And for digital designs we will simply use the SR model. And it turns out that this is realistic because in the digital designs that you have you seen and will be seeing in this course, the pull down MOSFET is on, or when these pull down MOSFETs are on, the output voltage is pulled down close to ground.

So vDS is very, very small.

So it does make sense that this model apply.

And when we talk about amplifiers, I am asking you to follow this discipline. I will tell you why in a second. I am saying analog designs follow this discipline that I call the saturation discipline.

It says simply operate the MOSFET operating in saturation as a current source. We will look at an amplifier in a second, and I will tell you why.

Now let's do a MOSFET amplifier.

Remember my amplifier had an input port and an output port.

And in general in our use we are going to have a common ground. And we have a VS and a ground here as well. That is the power port of the amplifier. The input port and the output port.

And let me redraw the circuit putting a MOSFET in place of the current source, RL, VS, vO, drain, gate, source, vI.

So my input is vI. Again, the MOSFET output is vO.

And I have a resistor RL. Hey, we've seen that before.

It turns out this is not surprising.

You've seen this before. This was our primitive inverter circuit. So what's different here?

We showed you the circuit as an inverter.

What's different here is that when we look at MOSFET behavior as a current source, this behaves like an amplifier.

In other words, when vDS is greater than some value then this behaves like a current source.

When vDS is small, in other words, in the digital design when vDS was small here, because when the MOSFET was on it pulled the voltage down to ground, we could view this behavior as a resistor.

And exactly the same thing, it is an amplifier.

And with digital designs, I was driving it with 5 volts and 0 volts and that was it, rail to rail.

As an amplifier, what I am doing now is looking at a small region of its behavior when vDS is greater than vGS minus VT. What I am saying is that for amplification let's follow the saturation discipline.

And the reason is that when this behaves like a current source, what I have shown you is that if this behaves like a current source I have shown you that this expression up here gives you amplification. In last lecture we plotted a bunch of values for vO versus vI, and we saw that we were getting amplification. For a small change in vI, I was getting a larger change in vO, and that was when I had the equation for a current source in there.

And so we know for a fact that if I can operate this as a current source, with a reasonable choice of values here, I am going to be able to get amplification.

What I haven't told you is if this is operated in the linear region, in fact, you do not get amplification.

I won't cover that, but you can check that out in your course notes as a discussion or you can try it out for yourself. Replace this with the SR model for small vDS and you can show yourselves that you don't get any amplification. In order to get the amplification we are telling ourselves let's focus on this part of the playground where vDS is greater than or equal to vGS minus VT. And for vGS greater than or equal to VT. So when vGS is greater than VT the MOSFET is on. Further, when vDS is large, larger than vGS minus VT this behaves like a current source.

So we have now created a small playground for ourselves where we can build lots of fun little amplifiers and other circuits.

And provided our circuits follow the saturation discipline where for the MOSFET or MOSFETs in the circuit these expressions are true then the MOSFETs are going to be in saturation, the current source model applies, and I will be indeed getting saturation. In future courses you may actually see the MOSFET used in other regimes of operation for a variety of reasons. But in 6.002 when we talk about amplifiers and so on we will be adopting the saturation discipline. And your homework problems and so on will state that. Assume that the MOSFETs are in saturation. What that means is that you can begin to model them as a current source and simply analyze their behavior accordingly. One minor nit.

Note that vDS for the MOSFET is the same as vO.

And vGS for the MOSFET is the same as vI.

So if you see me jumping back and forth using vOs and vIs or vDSs and vGSs they are the same thing in this circuit.

If you are dealing with circuits with many MOSFETs then you will have vDS1s and vGS1s and so on and so forth.

But for this simple circuit, vO and vDS are the same, vI and vGS are the same. So we could go ahead and analyze that circuit. What I do to analyze the circuit, I am telling you this. I am telling you that the MOSFET is behaving in saturation.

I am telling you this. We have disciplined ourselves to say that in that circuit the MOSFET is in saturation.

As soon as we tell you that we can then go ahead and analyze that circuit. And to analyze that circuit what you will do is simply replace the MOSFET with its equivalent model, and that looks like this.

Since you have been told that it is in saturation, we can replace the MOSFET with its current source model.

And the current iDS for the MOSFET is given by K/2(vI-VT)^2.

And it is always good to write the constraints under which you are implicitly working close by. So the constraints are one, vGS is greater than or equal to VT, vDS is greater than or equal to vGS minus VT. These constraints immediately follow from a statement of the type we are operating under the saturation discipline or the MOSFET is in saturation.

Let me just mark this equation as A, and we will refer to it again.

So with this new little circuit with the MOSFET working as a current source, let's go ahead and analyze our amplifier. Notice that to analyze the circuit I have a current source. It's a dependent current source where the

current depends on the square of the input.

So I want to go and analyze it. This is a nonlinear circuit.

So I can apply any one of the methods that we talked about last week for nonlinear circuits.

To analyze it I will go ahead and use the analytical method.

And my goal will be to obtain vO versus vI.

Again, remember where are we here?

The MOSFET circuit operating in saturation so I can replace this with a current source. It is nonlinear.

And so I can apply one of the two methods, the analytical method or the graphical method. Let's do both and start with the analytical method. The analytical method simply says go forth, apply the node method and solve. Simple stuff.

Let's go ahead and do that. Node method.

I have a single node here that is of interest.

I know the voltage vI at this node.

I know the voltage VS at this node.

So the only unknown is here at vO.

So I will go ahead and do that. Let me go ahead and equate the currents into the node to be zero.

So the currents out of the node here are iDS.

And that was equal the current into that same node.

So iDS must equal VS minus vO divided by RL.

iDS=VS-vO/RL. For later reference, let me call that B. Simplifying, what I can do is, we know that iDS is given by K/2(vI-VT)^2. So I replace iDS with this expression and I multiply that by RL.

So I get K/2(vI-VT)RL. So iDS gets multiplied by RL and I get vO on this side and VS remains out here.

All I have done is multiplied both sides by RL.

So it is RL iDS, taken RL iDS to this side, that is here, I get the minus sign, and VS stays here, vO comes here.

So that is my final expression. Remember this is true under certain conditions. I will keep hammering that home because some of the most common errors made by people is in forgetting the constraints under which this was obtained.

And the constraint under which this was obtained is the saturation discipline. And that was true when vGS for a MOSFET was greater than or equal to VT and vDS for a MOSFET was greater than or equal to vGS minus VT.

I also know that for vGS less than VT, vO=VS.

So when vGS is less than VT then this one turns off.

That's why it is the SCS model, switch current source model.

When vGS is less than zero it turns off and VS directly appears at vO. I would like to stare at this constraint with you for a second, vDS greater than or equal to vGS minus VT here. And vDS is simply vO.

I want to rewrite this constraint in terms of iDS.

It will come in handy. So iDS is K/2(vI-VT)^2.

This is vI-VT. So vI-VT is simply square root of 2iDS/K. In other words, I can write iDS less than or equal to K/2vO^2.

So this constraint expressed in terms of iDS is simply iDS less than or equal to K/2vO^2.

So all I've done here is analyzed this nonlinear circuit.

I can also analyze it using the graphical method.

And in order to do that, for my nonlinear circuit, in order to do that, all I have to do is plot.

Let's have iDS here and vDS here.

And as we did with a nonlinear expo dweeb, what I do is I plot the device characteristics iDS versus vDS.

The device characteristics under saturation look like this, so vGS increasing. iDS versus vDS has a bunch of curves that look like current sources of increasing values.

That simply reflects equation A.

And then I superimpose on top of that the expression that comes up due to equation B which is iDS equals, let me write that down here, iDS equals VS/RL - vO/RL.

That's B. And let me plot that.

That is a straight line relationship between iDS and vO.

And so when vO is zero iDS is VS/RL.

And when iDS is zero vO equals VS.

Remember, vO and vDS are the same.

So this is what I get. This is the straight line corresponding to equation B here.

And, as before, we just find the point where the two intersect. Let's say I am given some value of vGS. And let's say I am given some known value of vDS. So for that I can go ahead and find out the corresponding value of iDS from this graph.

Just as I told you when we did the expo dweeb stuff, this line here is called a load line.

You will be seeing that again and again and again where we have the equation corresponding to the one shown here, the equation written for the output loop superimposed on the device characteristics. That's called a load line.

So I can get this point corresponding to the operating point of the MOSFET for this iDS, vDS and vGS by using the graphical method. In the next lecture we are going to look at, given a device of this sort, how do we figure out the boundaries of valid operation so that the MOSFET stays in saturation?