Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2007

Lab 1: Thevenin/Norton Equivalents & Logic Gates
Handout S07-017

Introduction

The first part of the lab explores the characterization of a network by its Thevenin and Norton equivalents. The second part explores the static behavior of logic gates constructed with n-channel MOSFETs and resistors. You should complete the pre-lab exercises in your lab notebook before coming to lab. Then, carry out the in-lab exercises between February 26 and March 2. After completing the in-lab exercises, have a TA or LA check your work and sign your lab notebook. Finally, complete the post-lab exercises in your lab notebook, and turn in your lab notebook during recitation on Wednesday March 7.

Pre-Lab Exercises

Pre-Lab Exercises 1-1 and 1-2 explore the characterization of a network by its Thevenin and Norton equivalents. Pre-Lab Exercises 1-3 through 1-5 explore the static behavior of logic gates.

(1-1) Determine the Thevenin and Norton equivalents of the network shown in Figure 1 as viewed at its port.

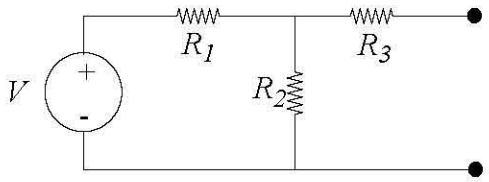

Figure 1: Source-resistor network for Pre-Lab Exercises 1-1 and 1-2.

(1-2) Evaluate the Thevenin and Norton equivalents of the network for the following values: $V = 5$ V; $R_1 = 50\ \Omega$; $R_2 = 2.2$ kΩ; $R_3 = 1.5$ kΩ.

(1-3) Figure 2 shows a NOT gate, a NOR gate, and a NAND gate constructed from n-channel MOSFETs and 1 kΩ resistors. The figure also shows a switch-resistor model for the n-channel MOSFET. Using the switch-resistor model, compute v_{OUT} for all three gates. In doing so, consider all combinations of input voltages; an input voltage may be either above or below the MOSFET threshold voltage V_{T}. In each case, evaluate v_{OUT} assuming $R_{\mathrm{DS-ON}} = 4\ \Omega$. Summarize your results for each gate in a table.

(1-4) Figure 3 shows a combinational logic circuit. Determine the input-output truth table for this circuit.

(1-5) Draw the circuit diagram for the combinational logic circuit shown in Figure 3 using the gates shown in Figure 2.

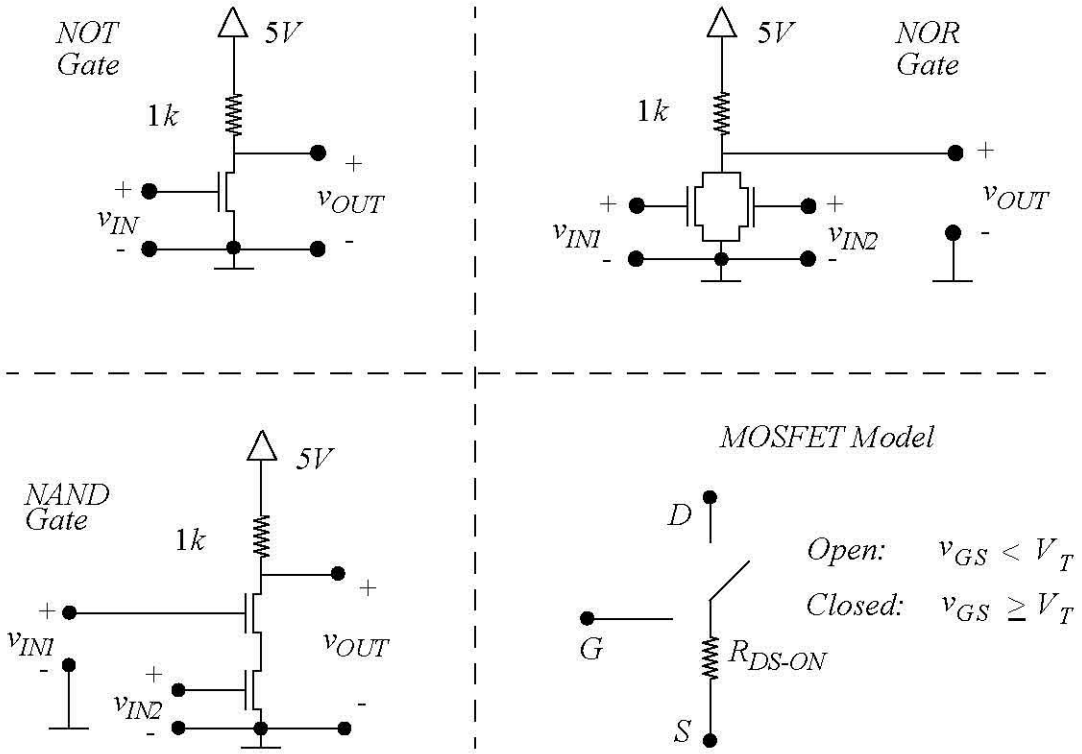

Figure 2: A NOT gate, a NOR gate, a NAND gate, and the switch-resistor MOSFET model.

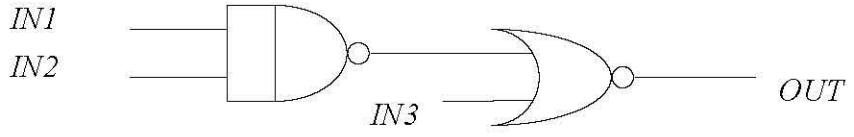

Figure 3: Combinational logic circuit for Pre-Lab Exercises 1-4 and 1-5.

In-Lab Exercises

In-Lab Exercises 1-1 through 1-3 explore the characterization of a network by its Thevenin and Norton equivalents. In-Lab exercises 1-4 through 1-9 explore the static behavior of logic gates.

(1-1) Construct the network shown in Figure 4. However, before connecting the signal generator to the remainder of the network, set its output voltage to a constant 5 V, and check this output with the multi-meter. The network is the same as the one shown in Figure 1, with the function generator serving as both the voltage source and resistor R_1. *Note: The function generator has two modes to compensate for the load impedance– 50 Ω and High Z. Make sure that your function generator is set to the High Z mode. Press [Shift] and then [Enter] to get to the menus. Using the dial, switch to menu D, the SYS MENU. Next press the down arrow twice. Use the dial to switch to HIGH Z. Then press [Enter] to save.*

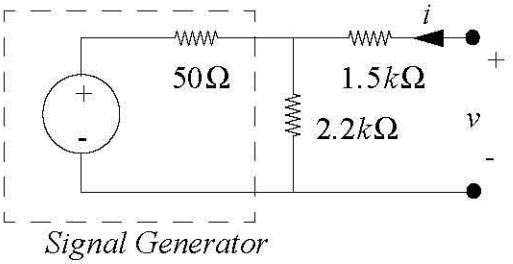

Figure 4: Experimental source-resistor network.

(1-2) Measure the open-circuit voltage and short-circuit current of the network with the multi-meter. Note that the multi-meter is itself a near open circuit when used as a voltmeter, and a near short circuit when used as an ammeter. Therefore, the direct connection of the multi-meter across the port implements the proper measurement in both cases. Your results from Pre-Lab Exercise 1-2 should show that both measurements are within the safe range for the multi-meter.

(1-3) Connect a resistor across the network port and measure the port voltage v with the multi-meter. Do so for resistors having resistances of 560 Ω, 1 kΩ and 2.2 kΩ.

(1-4) Construct the circuit shown in Figure 5, which is designed to measure the threshold voltage of the MOSFET; the MOSFET pin assignments are given in the attached data sheet. The MOSFET should say 2N7000 on it. Make sure that you don't accidentally reverse the polarity of the MOSFET. The source should be connected to ground, and the drain to the 1 kΩ resistor. (As evident from the MOSFET schematic in the datasheet, note that the drain and source terminals of discrete MOSFETs are not symmetric). Use the multi-meter to measure v_{GS} and the oscilloscope to measure v_{DS}, and set the signal generator to provide a constant output. With v_{GS} at 0 V, v_{DS} should be at 5 V. Gradually increase v_{GS} until v_{DS} starts to fall. The value of v_{GS} at which this occurs is V_T.

(1-5) Beginning with the circuit shown in Figure 5, remove the 1 kΩ resistor and the oscilloscope from the MOSFET drain. With v_{GS} at 5 V, measure R_{DS} with the multi-meter. This resistance is R_{DS-ON} for $v_{GS} = 5$ V; note that the multi-meter supplies a very small voltage when used as an ohmmeter.

(1-6) Construct the NOT gate from Figure 2 and connect its input to a switch and 10 kΩ resistor

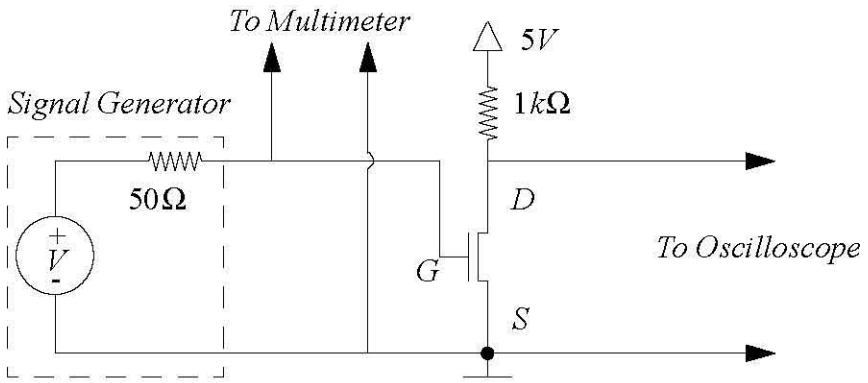

Figure 5: Circuit to measure V_T.

as shown in Figure 6. For both switch positions, that is for both logic input levels to the gate, measure v_{OUT} with the multi-meter.

A switch pack and a 10 kΩ resistor array (10k SIP pn.A103J) have been chosen to simplify the wiring of the switches to their associated resistors. Specifically, the switch pack can be placed in the protoboard so that one side is on a common ground strip and each pin on the other side is on a separate trace. Then, the resistor array can be inserted into the protoboard along side the switch pack so that separate resistors connect to each switch. Finally, the common pin of the resistor pack, designated by the white circle, can be connected to the 5 V power supply through a single wire. A diagram of this setup is seen in Figure 7.

(1-7) Construct the NOR gate from Figure 2. As for the NOT gate shown in Figure 6, connect the inputs to the NOR gate to switches and 10 kΩ resistors. For all combinations of switch positions, that is for all combinations of logic input levels to the gate, measure v_{OUT} with the multi-meter. *Save the NOR gate for In-Lab Exercise 1-9.*

(1-8) Repeat In-Lab Exercise 1-7 for the NAND gate. *Save the NAND gate for In-Lab Exercise 1-9.*

(1-9) Use the NOR gate and NAND gate to implement the combinational logic circuit of Figure 3, as outlined in Pre-Lab Exercise 1-5. Connect each input to a switch and resistor as in In-Lab Exercises 1-6 through 1-8. By changing its input switch settings, and measuring its output voltage with the multi-meter, demonstrate that the logic circuit functions properly.

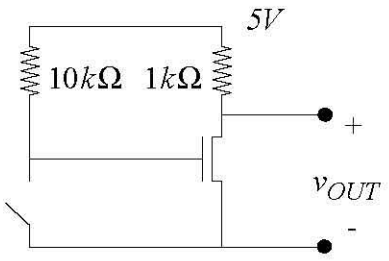

Figure 6: Experimental NOT gate.

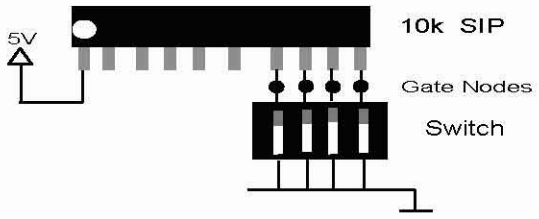

Figure 7: Switch pack and resistor array setup

Post-Lab Exercises

Post-Lab Exercises 1-1 through 1-3 explore the characterization of a network by its Thevenin and Norton equivalents. Post-Lab Exercises 1-4 and 1-5 explore the static behavior of MOSFETS and logic gates.

(1-1) Refer to your measurements from In-Lab Exercise 1-2; note that these measurements are the Thevenin equivalent voltage and Norton equivalent current of the network in Figure 4. From these measurements, compute the Thevenin/Norton equivalent resistance of the network. Compare the experimental Thevenin/Norton parameters to their corresponding values from Pre-Lab Exercise 1-2, and explain any discrepancies. Hint: consider measurement error and resistance variation.

(1-2) Refer to your measurements from In-Lab Exercise 1-3. For each combination of resistor and voltage measurement, calculate the corresponding port current i.

(1-3) Using the open-circuit voltage and short-circuit current measured during In-Lab Exercise 1-2, graph the i-v relation for the network. On this graph also plot the i-v data obtained by combining the voltages measured during In-Lab Exercise 1-3 and the currents calculated during Post-Lab Exercise 1-2. Explain any discrepancies between the measured i-v data and the i-v relation obtained from the Thevenin/Norton parameters.

(1-4) Consult the MOSFET data sheet and determine $R_{\mathrm{DS-ON}}$ and V_{T}, respectively. Compare these to the values you measured during In-Lab Exercises 1-5 and 1-4, respectively.

(1-5) Using the value of $R_{\mathrm{DS-ON}}$ measured during In-Lab Exercise 1-5, re-calculate the output voltages calculated in Pre-Lab Exercise 1-3. Explain any discrepancies between the re-calculated output voltages and those measured during In-Lab Exercises 1-6 through 1-8.

(1-6) Using the measured values of $R_{\mathrm{DS-ON}}$ and V_{T} for the inverter that you built, specify values for V_{OL}, V_{IL}, V_{OH}, and V_{IH} that achieve the best *symmetric* noise margins. (See Section 5.1, page 245 and Section 6.8, page 306, of the course text).